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Device Physics and Device Mechanics for Flexible MoS_2 Thin Film Transistors

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Device Physics and Device Mechanics for Flexible MoS_2 Thin Film Transistors

by

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Dedication

This is dedicated to my parents for endless love and support

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Finally, special thanks should go to my family – My mother, father, brother, grandmother, aunts and uncles. Thank them for their generous supports and unconditional love. None of anything I have achieved would have been possible without them.

Device Physics and Device Mechanics for Flexible MoS_2 Thin Film Transistors

Hsiao-Yu Chang, Ph.D.

The University of Texas at Austin, 2015

Supervisor: Deji Akinwande, Nanshu Lu

While there has been increasing studies of MoS_2 and other two-dimensional (2D) semiconducting dichalcogenides on hard conventional substrates, experimental or analytical studies on flexible substrates has been very limited so far, even though these 2D crystals are understood to have greater prospects for flexible smart systems. In the first part, we report detailed studies of MoS_2 transistors on industrial plastic sheets. Failure mechanisms under strain are studied with bending test and stretching test. Experimental investigation identifies that crack formation in the dielectric and the buckling delamination in MoS_2 are responsible for the degradation of the device performance. Several approaches to improve device flexibility were discussed. In the second part, electronic transport properties in multilayer MoS_2 are investigated with Y-function method. By combining experiments and analysis, we show that the Y-function method offers a robust route for evaluating the low-field mobility, threshold voltage and contact resistance even when the contact is a Schottky-barrier as is common in two-dimensional transistors. In addition, an independent transfer length method (TLM) evaluation corroborates

the modified Y-function analysis. The last part, we demonstrate the first RF performance for transferred CVD-grown MoS_2 FETs on the flexible substrate. Our result suggests that the large-area CVD-grown MoS_2 provides a practical route to realize low-power, high speed electronics circuit applications in the future.

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Chapter 1. Introduction

Applications of flexible electronics

Future ubiquitous smart electronic systems are envisioned to afford arbitrary form factors, robust elasticity, high speed charge transport, and low-power consumption - a combined set of attributes which demonstrate uniform electronic properties across a wide range of applied strains.[7-9] We are interested in integrating the smart system on different substrates. Once we can replace the substrate, many unique applications will appear that the conventional silicon may not be able to realize. For example, when the substrate becomes transparent, we can make the smart glass (Figure 1.1a). When the substrate becomes flexible, we can make the bendable, stretchable or even foldable devices. We can make the electronic-paper (Figure 1.1b), or apply it toward biomedical applications. Figure 1.1c shows a biosensor which can be attached on our body. These sensors can transfer our health signals to the center monitoring system through wireless communication, so once something wrong happens in our body, the center monitoring system can respond in a timely manner and take care of the emergency situation. As described in Figure 1.1d, this is how the home healthcare monitoring system works. Allowing for the extension of substrates can lead to very promising applications related to internet of things (IoT).

For flexible electronics, high performance, transparence and the flexibility, these three properties are all important for this application area, but we may not need to have them all in one all the time. Each requirement depends on the application. In this study, we mainly focus on the device performance, and their mechanical properties.

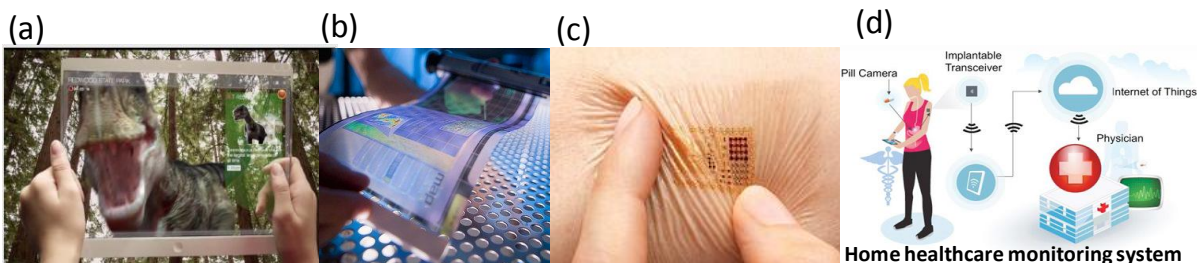

Figure 1.1. (a) Smart glass (from Corning), (b) Electronic-paper (from Arizona State University and HP), (c) Medical sensor (from MC10), (d) Home healthcare monitoring system (from N2M Advisory).

Survey of flexible substrates

The selection of substrate is critical to enable the device to be flexible, reliable and comparable to the fabrication process. As shown in Figure 1.2, there are several options such as polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polycarbonate (PC), polyimide (PI) and willow glass. The maximum process temperature constraints will be limited by the glass transition temperature provided by the substrate. Although willow glass can provide the highest processing temperature compared to other options, it is still glass, so it is still brittle with limited flexibility. To gain this additional 100℃by selecting willow glass, we will sacrifice the flexibility a lot. Besides this, the surface roughness, and chemical resistance are all important for the process requirement. In this study, we chose polyimide since it can meet all our process requirements.

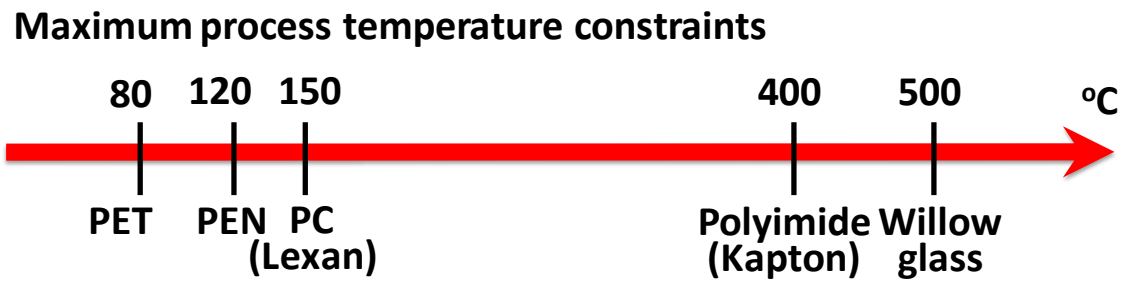

Figure 1.2. Maximum process temperature constraints of several different plastic substrates.

Why 2D materials for flexible electronics?

A major contemporary challenge concerns the choice of the semiconducting material suitable for high-performance field-effect transistors (FETs) on a flexible substrate.[7, 8, 10] Using pliable electronic materials, such as semiconducting polymers and organic molecules, to fabricate thin-film transistors (TFTs) on soft substrates has had limited applications due to the low field-effect mobilities[7, 11, 12]. Enhanced device performance has been achieved by utilizing thin films of conventional semiconductor materials, including crystalline and polycrystalline Si and III-V semiconductors that offer improved electronic properties albeit at the cost of overall device flexibility and thickness scalability[1, 13-15]. More recently, graphene has attracted substantial interest for high-performance flexible electronics owing to its high carrier mobility (>10,000 cm^2/V-s) and outstanding radio-frequency properties,[16-21] however, its lack of a bandgap is a major drawback since low-power switching or digital transistors cannot be realized.[22] This drawback has consequently motivated the search for other layered atomic sheets with substantial bandgaps such as the semiconducting transition metal dichalcogenides (TMDs).[23, 24] Molybdenum disulfide (MoS_2) is a prototypical TMD that has been attracting rapidly growing

interest owing to its large semiconducting bandgap (~1.8 eV for monolayer and ~1.3 eV for bulk films), which is ideal for low-power electronics on hard and soft substrates.[23, 25-29] In addition, its high carrier mobility (170 cm^2/V-s at room temperature),[30] high strength,[31] and large surface to volume ratio make it a compelling semiconducting nanomaterial for high speed flexible transistors and sensors.

Among different kinds of 2D materials, graphene offers the fastest charge transport, stiffness, and thermal conductivity. Molybdenum disulfide (MoS_2), phosphorene, and other semiconducting transition metal dichalcogenides (TMDs) are suitable for digital electronics. In addition, direct bandgap TMDs can be used for optoelectronics. In addition to electronic properties, 2D materials possess clear advantages, both in the scalability to ultra-thin layer and elastic limit. In comparison with traditional semiconductors for flexible nanoelectronics, 2D materials demonstrate high electronic performance as well as high flexibility (see Figure 1.3).[1]

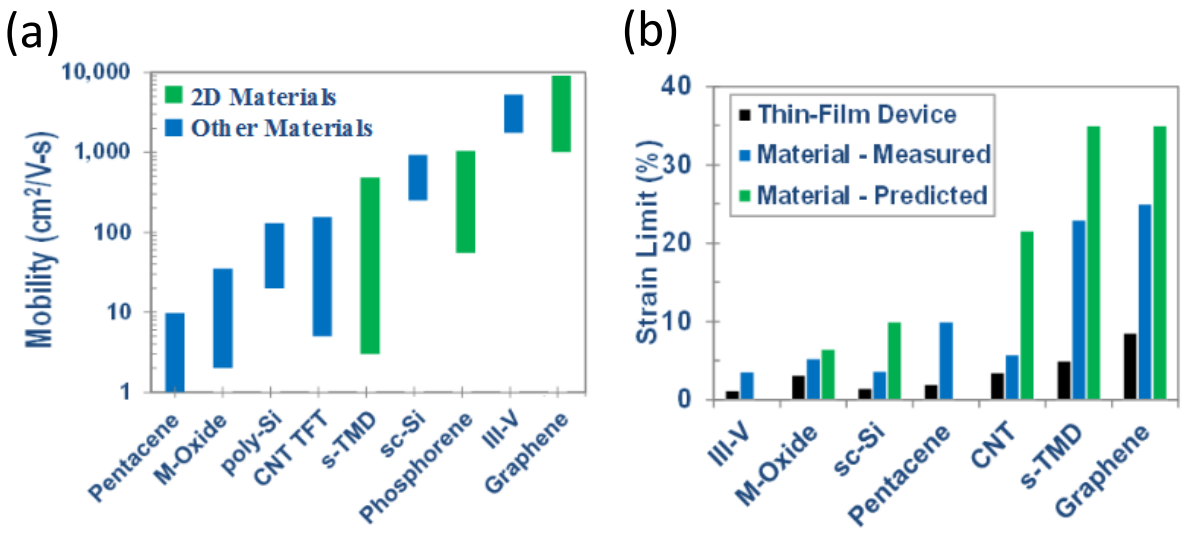

Figure 1.3. [1] Mobility and strain comparison of candidate materials for flexible TFTs. (a) Comparison of experimentally reported FET mobilities of candidate synthetic materials for flexible TFTs, including mobility variations reported across a wide variety of experimental

samples at room temperature. **(b)**. Maximum elastic strain limits of candidate materials for flexible TFTs. 2D materials offer higher theoretical and measured strain limits than conventional bulk semiconductor materials.

Chapter 2. Fabrication and characterization of MoS_2 devices

Device fabrication and material characterization

For the flexible devices, we used commercially available polyimide (Kapton) with a thickness of 76 μm as the flexible substrate, and spin-coated an additional liquid polyimide film (PI-2574 from HD Micro Systems) on the surface with a thickness of 26 μm to reduce the surface roughness. The liquid polyimide was cured at 300 °C for 1 hour. Ti/Pd (2/50 nm) deposited by electron beam evaporation was used as the bottom gate electrode, and Al_2O_3 or HfO_2 (25 nm) deposited at 200 °C by atomic layer deposition (ALD) method as the gate dielectric. Due to the present challenge of synthesizing high-quality continuous layers of MoS_2 uniformly across a substrate,[32-34] MoS_2 devices were prepared by mechanical exfoliation from commercial crystals (SPI supplies) onto the flexible substrate for this study. Flakes with thickness between 7.9-23.5 nm were selected by optical microscope and confirmed by atomic force microscope (AFM). Source/drain contacts were defined by electron beam lithography, and Ti/Au (2/50 nm) were deposited by electron beam evaporation followed by the lift off process.

In addition to the flexible devices, we also made MoS_2 devices on rigid substrates. Highly doped Si substrate was used as the bottom gate, and 270 nm SiO_2 deposited by thermal oxidation or 25 nm Al_2O_3 by ALD method was used as the gate dielectric. The remained steps are the same as the flexible samples. Channel length is fixed to 1 μm, except for the device structures of transfer length method (TLM), while channel width is determined by the width of each flake, typically in the range of 0.7~4 μm.

Figure 2.1a shows the AFM analysis for a MoS_2 flake with thickness of around 15 nm. The Raman spectroscopy (Figure 2.1b) shows the peak spacing between the E^1_{2g} and A^1_g vibration mode is 25 cm^{-1}, which indicates that the flake has four or more layers.[3] Focused ion-beam (FIB) was used to prepare a cross-section transmission electron microscopy (TEM) sample (Figure 2.1c), which shows that the interlayer spacing of MoS_2 is around 6.5 Å, and defects can sometimes be found in the exfoliated MoS_2 crystal. Figure 2.1d and e show the schematic depiction and the optical microscope image of the MoS_2 device made on polyimide. Figure 2.1f displays the photograph of the fabricated flexible sample.

Material characterization: Renishaw In-Via Raman Microscope with He-Cd blue laser (442 nm wavelength) was employed for the Raman spectroscopy of MoS_2 samples. A Veeco tapping-mode atomic force microscope was used for thickness, morphology and surface analysis.

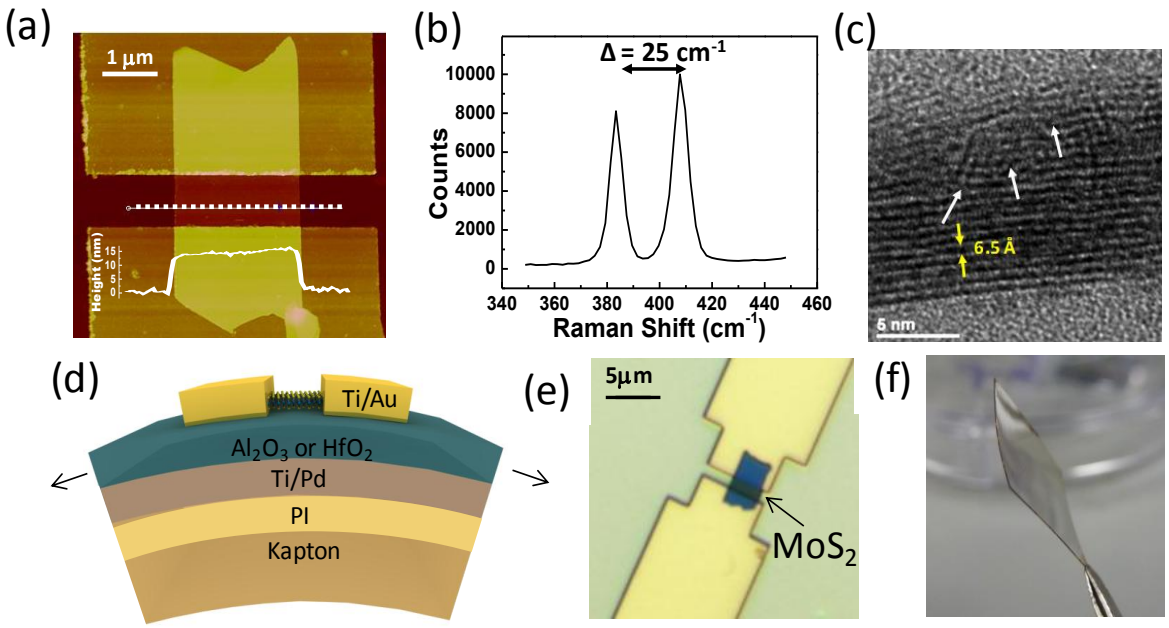

Figure 2.1. [2] (a) AFM analysis shows the thickness of a MoS_2 flake which is around 15 nm. The height profile of MoS_2 flake is scanned along the dotted line. (b) From the Raman spectrum of the MoS_2 flake, the peak spacing between the E^1_{2g} and A^1_g vibration mode is 25 cm^{-1} confirming that the MoS_2 flake is a multi-layer film.[3] (c) TEM image of multi-layer MoS_2 showing the layered nature with interlayer spacing of around 6.5 Å. Point and line defects can be found in the exfoliated MoS_2 crystal, which are marked by arrows. MoS_2 flakes were exfoliated onto SiO_2/Si and then covered with epoxy for cross-sectional imaging. (d) The schematic depiction of the flexible bottom gate device structure. (e) The optical microscope picture for the MoS_2 device after the S/D patterned by e-beam lithography. The channel length is 1 μm and the MoS_2 flake with thickness of around 10 nm shows dark blue color in the optical image. (f) The photograph of the flexible sample made on industrial polyimide sheet with cured liquid PI on the surface (total thickness is ~102 μm).

Device studies

Electrical characteristics of the flexible MoS_2 FETs were then evaluated under ambient conditions. Representative transfer (I_D-V_G) characteristics are shown in Figure 2.2a and b. The extracted low-field mobility of the fastest device is 30 cm^2/V-s (Figure 2.2c) using the Y-function method which is defined as $I_D/\sqrt{g_m}$ (I_D is the drain current, g_m is the transconductance) and is especially suitable for studying device physics because it excludes the contact resistance effect on the mobility.[35, 36] The details of the mobility extraction will be provided in Chapter 3.1. The ON/OFF switching ratio is more than 10^7, and the sub-threshold slope is ~82 mV/decade. Output (I_D-V_D) characteristics shows negligible Schottky barrier in the linear region, and current

saturation at high fields as shown in Figure 2.2d. These device characteristics represent the state-of-the-art for MoS_2 FETs on flexible substrates, with 4x higher mobility and >100x greater ON/OFF ratio compared to a previously reported MoS_2 device.[29] These results are comparable with unpassivated MoS_2 FETs realized on Si substrates,[25, 37] indicating that its unique electrical properties can be accessed on hard and soft substrates alike which is a welcome benefit for flexible electronics. Further improvement of the device performance can be achieved by mobility enhancement through passivation with a high-k dielectric to enhance the local screening effect and suppress Coulomb scattering as previously reported,[25, 37-39] and reducing the contact resistance by using low work function metals, such as Scandium, to minimize the Schottky barrier at the contact.[40] However, for flexible MoS_2, the device passivation entails further research beyond what has been achieved on hard substrates, requiring not just the investigation of dielectric films with high-permittivity but also consideration of its mechanical properties in order to ensure no detrimental impact to device flexibility and elasticity as we will elucidate subsequently. This will involve investigation of the parameter space of the passivation material including thickness, stiffness, permittivity and adhesion to the TMD to prevent delamination or early cracking under deformation.

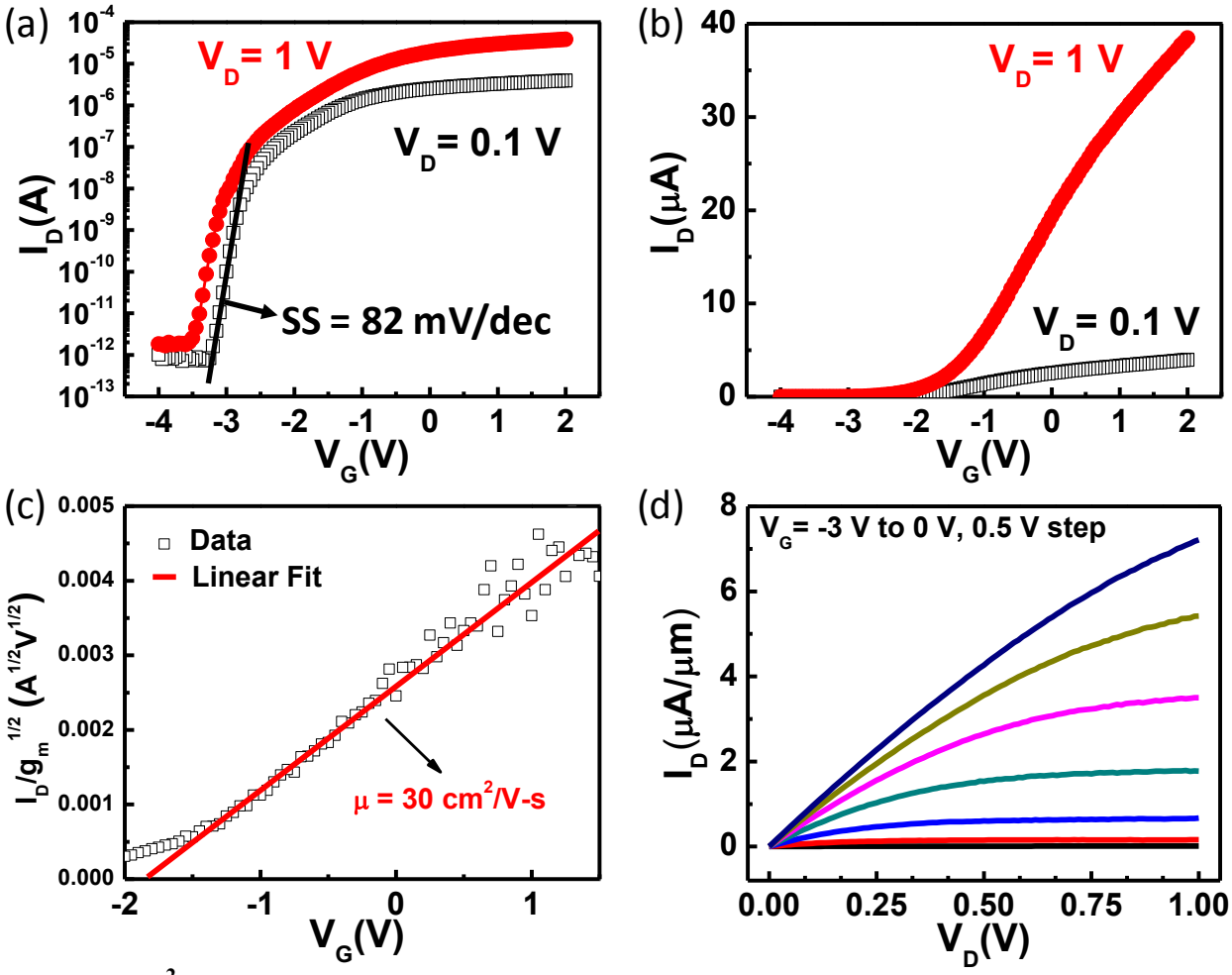

Figure 2.2. [2] A representative MoS_2 FET (W/L = 3/1 μm) made with Al_2O_3 as gate dielectric on flexible PI. (a) I_D-V_G characteristics in log scale. The ON/OFF current ratio is more than 7 orders of magnitude, and the sub-threshold slope (SS) is ~82 mV/decade. (b) I_D-V_G characteristics in linear scale. (c) The experimental Y-function (=$I_D/\sqrt{g_m}$) profile showing the characteristic linear profile for extracting the low-field mobility. The extracted low-field mobility is 30 cm^2/V-s. (d) I_D-V_D characteristics indicates negligible Schottky barrier in the linear region, and current saturation at high fields.

Supplementary information

Hysteresis of MoS_2 devices

The hysteresis of a representative MoS_2 device are around 520 mV and 350 mV for V_D=0.1 V and 1 V respectively. These values are due to the unpassivated devices measured in atmosphere.

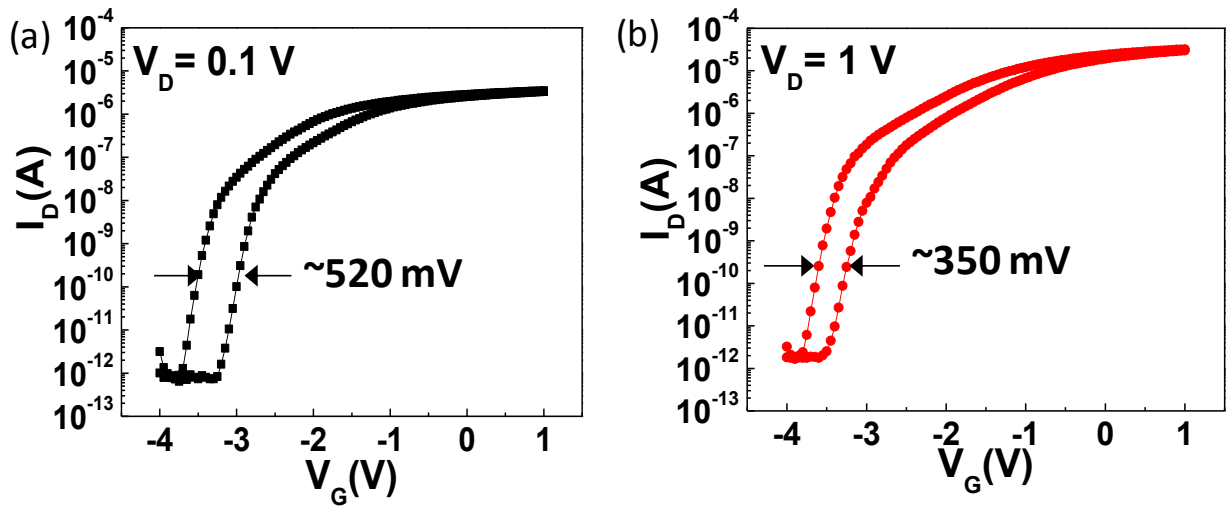

Figure 2.3. [[2]] Hysteresis of a representative MoS_2 device. This is the same device reported in Figure 2 of the main text. (a) Vd=0.1V, (b) Vd=1V.

The thickness dependence of the electron mobility

Based on our experimental devices within the thickness range of 7.9-21 nm, the maximum mobility occurs for a thickness of 7.9 nm, and decreases as the thickness increases. Our devices show the same trend of mobility dependence on thickness as the previous report.[40] (See Figure

2.4 shown below). The thickness dependence down to very thin MoS_2 is not known due to the poor optical contrast in identifying thin flakes. The scattered data is attributed to several effects including the variation of crystal orientation with respect to the conducting direction, the presence of defects, uncontrolled impurity contamination from the exfoliation process, the width and edge morphology of the flakes, etc. This issue requires further studies particularly on flexible substrates and will be a focus of future comprehensive research.

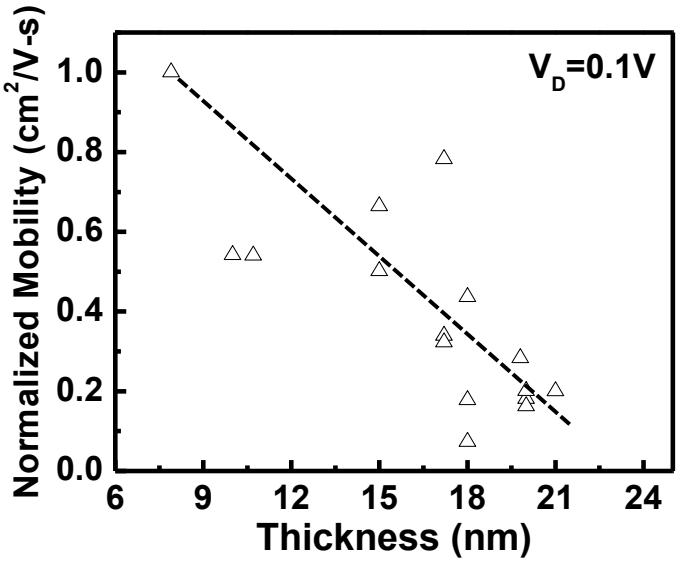

Figure 2.4. [2] The thickness of MoS_2 versus normalized electron mobility. The mobility was normalized to the maximum mobility observed within these devices. The thickness was confirmed by AFM analysis. The dashed line is a visual guide indicating a general inverse dependence.

Device characteristics with HfO_2 as gate dielectric

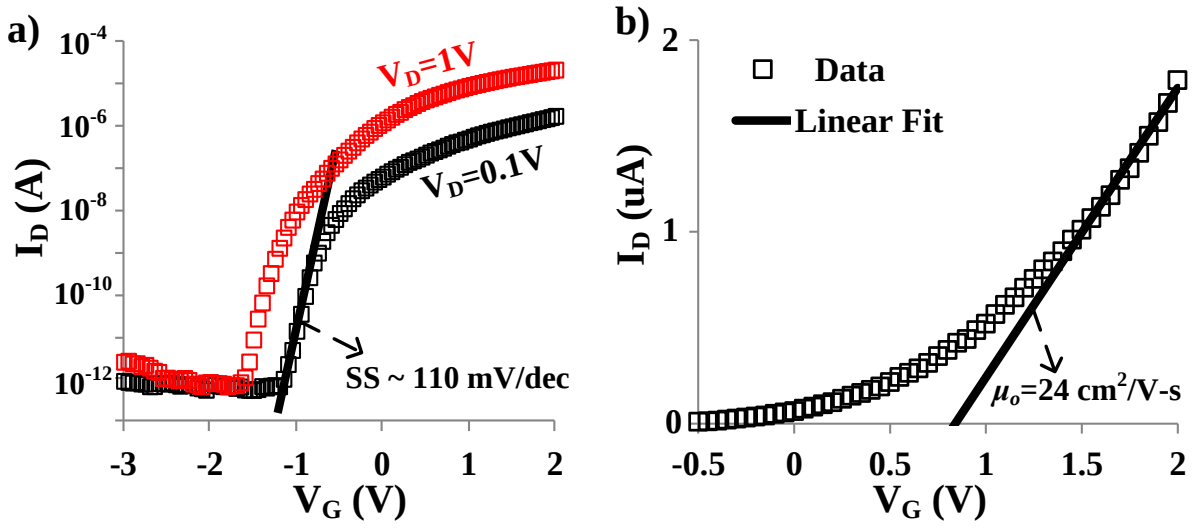

Figure 2.5. [2] A representative MoS_2 FET made with HfO_2 as gate dielectric on flexible PI. (a) I_D-V_G characteristics in log scale. (b) I_D-V_G characteristics in linear scale with an extracted low-field mobility of 24 cm^2/V-s. Device W/L = 1.25/1 μm.

The intrinsic gain (g_m/g_{ds})

The intrinsic gain (g_m/g_{ds}) is above 100 at V_D=0.5 V which is extracted in the current saturation region.

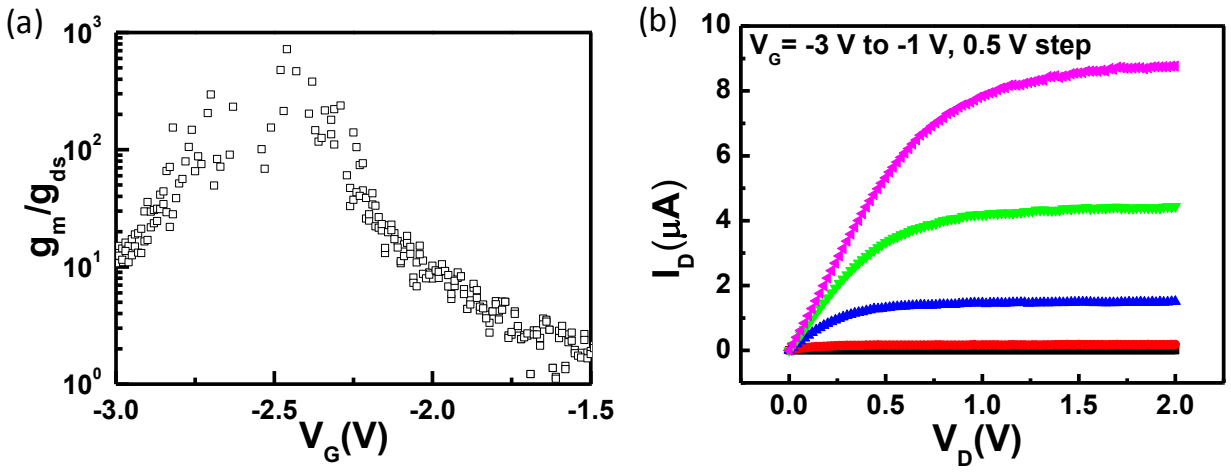

Figure 2.6. [2] (a) The intrinsic gain (g_m/g_{ds}) is above 100 at V_D=0.5 V. (b) I_D-V_D characteristics show that the intrinsic gain is extracted in the current saturation region. Device W/L = 3/1 μm.

Chapter 3. Y-function method for extracting mobility and contact resistance

Introduction to the Y-function method

The major challenge in understanding the intrinsic charge transport properties arises from the substantial R_c that is typical of metal interfaces to low-dimensional systems such as 2D atomic layers,[28, 41-43] which is often a Schottky-barrier interface when the 2D layer is a semiconductor as is the case for MoS_2, and similar TMDs. As a result, established methods based on the transconductance or two-point conductance of field-effect devices can result in mobility underestimation in the presence of typical R_c profile, which is either gate independent (Ohmic contact) or inversely proportional to the magnitude of the gate voltage (Schottky contact). In the unusual case of R_c that is directly proportional to gate voltage, we show later that mobility overestimation can even occur. While this challenge has been long recognized, and indeed discussed in the first reports of (1D) carbon nanotube transistor devices (in 1998),[44] there remains a need for a routine technique that can decouple the mobility evaluation from the contact resistance and yield accurate estimates for both, particularly for understanding the properties and prospects of semiconducting atomic crystals based on TMDs, which has only recently attracted broad attention.[45]

In this chapter, we show that the so-called (Ghibaudo) Y-function method,[35] can be modified to include a gate dependent Schottky-barrier and afford robust evaluation of the low-field carrier mobility in experimental MoS_2 transistors. In addition, the threshold voltage and effective contact resistance in large gate overdrive bias condition can be simultaneously extracted from the

same Y-function analysis. In addition, an independent transfer length method (TLM) evaluation further corroborates the Schottky-barrier R_c and modified Y-function analysis.

For the experimental study, we employed highly doped Si substrate as the bottom gate, and deposited either 270 nm SiO_2 by thermal oxidation or 25 nm Al_2O_3 by atomic layer deposition (ALD) method as the gate dielectric. The channel material, MoS_2, was prepared by mechanical exfoliation from commercial crystals (SPI supplies). Flakes with thickness below 22 nm were selected by optical microscope and confirmed by atomic force microscope (AFM). Source/drain contacts were defined by electron beam lithography, and Au (50 nm) or Ti/Au (2 nm/50 nm) were deposited by electron beam evaporation followed by the lift-off process. Channel length is fixed to 1 μm, except for TLM device structures, while channel width is determined by the width of each flake, typically in the range of 0.7~4 μm. The transmission electron microscopy (TEM) sample (Figure 2.1c), which shows that the interlayer spacing of MoS_2 is around 6.5 Å, and defects can sometimes be found in the exfoliated MoS_2 crystal. This implies that even though the TLM structure is made on the same flake, local defects can play a noticeable role that can result in individual differences.

Electrical characteristics of the fabricated MoS_2 FETs were then evaluated and analyzed by the Y-function method[35] which was first proposed by Ghibaudo for low-field mobility (μ_o) and threshold voltage (V_T) extraction in Si transistor devices for its accuracy and simplicity considering first-order mobility attenuation coefficient and constant contact resistance. We show in the latter half of this article that the Y-function method remains robust and accurate even in the presence of gate voltage dependent (Schottky-barrier) contact resistance, which is typical for FETs based on TMDs. [46-49]

The Y-function method is based on the straightforward analysis of the drain current (I_D) in the linear region. Considering that Schottky-barrier induced contact resistance at source and drain end will result in additional voltage drops, the I-V equation can be expressed as[50]

$$I_D = \left(\frac{\mu_o}{1+\theta_o(V_G - V_T)} \right) C_{ox} \frac{W}{L} (V_G - V_T - 0.5V_D)(V_D - I_D R_c) \quad (1)$$

where first-order mobility attenuation coefficient, θ_o, introduced by remote phonon scattering and surface roughness is included to better depict the realistic device performance.[5] C_{ox} is the gate capacitance, and W and L are the device width and length respectively. V_G and V_D are the gate and drain voltages, respectively. L = 1 μm, and V_D = 0.1 V was chosen to evaluate the mobility in the low-field bias condition. In the low-field limit, V_G-V_T >> $0.5V_D$ under large gate overdrive, hence, the $0.5V_D$ factor can be ignored to further simplify Equation (1). For convenience, we combine both θ_o and R_c effects as one effective mobility attenuation factor, $\theta = \theta_o + \mu_o C_{ox} R_c W/L$. Therefore, Equation (1) can be rewritten as

$$I_D = \left(\frac{\mu_o}{1+\theta(V_G - V_T)} \right) C_{ox} \frac{W}{L} (V_G - V_T) V_D \quad (2)$$

The Y-function is defined as $I_D/\sqrt{g_m}$, where g_m is the transconductance defined as dI_D/dV_G. Due to the existence of Schottky-barriers at the source and drain contact, we consider the case where R_c is also V_G dependent when calculating dI_D/dV_G. It follows that in the general case, the Y-function is given by

$$Y = \frac{I_D}{\sqrt{g_m}} = \frac{\sqrt{\mu_o C_{ox} V_D \frac{W}{L}}}{\sqrt{1 - \mu_o C_{ox} R_c' \frac{W}{L}(V_G - V_T)^2}}(V_G - V_T) \quad (3)$$

where R_c' is dR_c/dV_G . We first assume that R_c is not V_G dependent, resulting in the simplified expression Y = $(\mu_o C_{ox} V_D W/L)^{0.5}(V_G\text{-}V_T)$ for the extraction of the low-field mobility and the threshold voltage.[35] Subsequently, we will examine the validation of this assumption afterwards in order to understand the impact of voltage dependent R_c on mobility extraction.

Figure 3.1a-c is a representative example for extracting μ_o, V_T, and R_c of an experimental MoS_2 FET from the simplified Y-function. First, we plot the Y-function with respect to V_G as shown in Figure 3.1a. From the linear fit in large gate overdrive region, V_T = -32.1 V and μ_o = 55.7 cm^2/V-s can be extracted from the x-intercept and the slope respectively, given that the capacitance of the gate dielectrics used in this work were measured separately by standard C-V techniques on fabricated test structures. Strong agreement to a linear profile is observed. Figure 3.1b shows θ versus V_G. In the absence of estimates for θ_o, which is the case for MoS_2, an upper bound can be placed on R_c in the limit of negligible θ_o. With $\theta \approx \mu_o C_{ox} R_c W/L$, $R_c \approx$ 20.4 Ω-mm is extracted from the large gate overdrive region. Figure 3.1c shows the transfer characteristic (I_D-V_G) for MoS_2 FET in both log and linear scales. ON/OFF switching ratio is ~10^7 at V_D = 0.1 V from the log scale, and the model (Equation (2)) offers strong agreement to the experimental data shown in the linear scale.

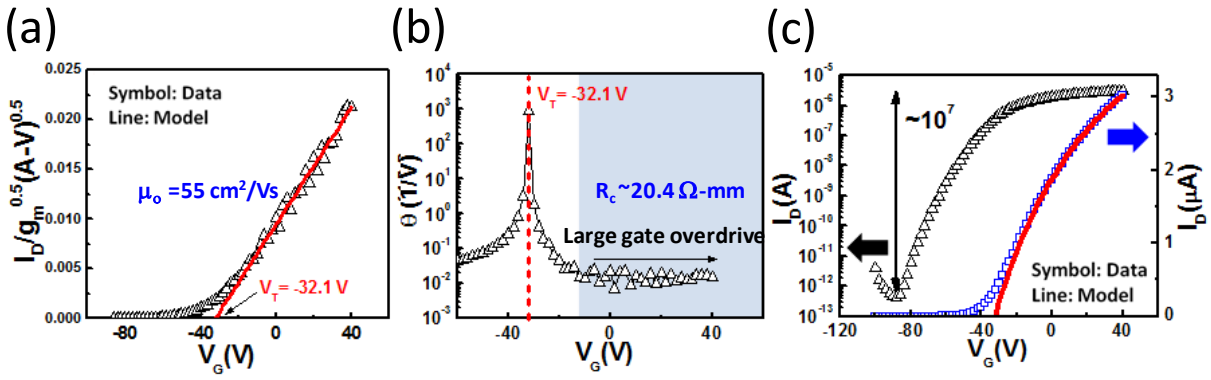

Figure 3.1. [4] (a) MoS_2 FET fabricated with 270 nm SiO_2 as gate dielectric, and 50 nm Au as S/D metal. From the linear fitting in the large gate overdrive region, which shows good agreement, both V_T = -32.1 V and μ_o = 55.7 cm^2/V-s can be extracted from the x-intercept and the slope respectively. The insert is a schematic depiction of the bottom-gate MoS_2 device. (b) With $\theta \sim \mu_o C_{ox} R_c W/L$, $R_c \sim$ 20.4 Ω-mm is extracted from the large gate overdrive region. (c) The transfer characteristic (I_D-V_G) for MoS_2 FET in both log and linear scales at V_D = 0.1 V. The model shows strong agreement to the experimental data.

Mobility underestimation from maximum g_m

Arguably, the most common method typically chosen to extract the field-effect mobility is from the maximum or peak transconductance ($g_m = \mu_{FE} C_{ox} V_D W/L$, where μ_{FE} is the field-effect mobility extracted from g_m) in the transistor linear region. However, this extracted mobility (μ_{FE}) can significantly underestimate the true low-field mobility (μ_o) in the presence of substantial contact resistance. In the large gate overdrive region, we can derive the dependence of the

mobility underestimation error as a function of the normalized contact resistance (R_c/R_{tot}), which can be expressed as,

$$\frac{\mu_{FE}-\mu_o}{\mu_o}=(\frac{R_c}{R_{tot}})(\frac{R_c}{R_{tot}}-2) \quad (4)$$

We note that the total (channel plus contact) resistance, $R_{tot} = V_D/I_D$ is a function of V_G-$V_{T,}$ and so is μ_{FE}. With Equation (4) (which is ≈ -2R_c/R_{tot} when R_c/R_{tot} << 2), we can quantitatively estimate the mobility underestimation error arising from finite contact resistance. Figure 3.2 shows device statistics of the mobility underestimation from μ_{FE} extracted from g_m and $g_{m,max}$ compared to μ_o extracted from the Y-function as a function of the significance of the contact resistance (R_c/R_{tot}). Data extracted from nineteen devices made on 270 nm SiO_2 as the gate dielectric and Ti/Au or Au as the contact metal show strong agreement with the model in the large gate overdrive region. However, for devices with larger R_c, $g_{m,max}$ happened at small gate overdrive which is outside (not fully applicable for) the fitting range of the Y-function. As a result, the extraction from $g_{m,max}$ gives additional underestimation of μ_o due to this deviation from the model. For 16 out of the 19 devices in our statistics, R_c/R_{tot} is in the range of 7-23 % corresponding to the mobility underestimation of 15-60 %.

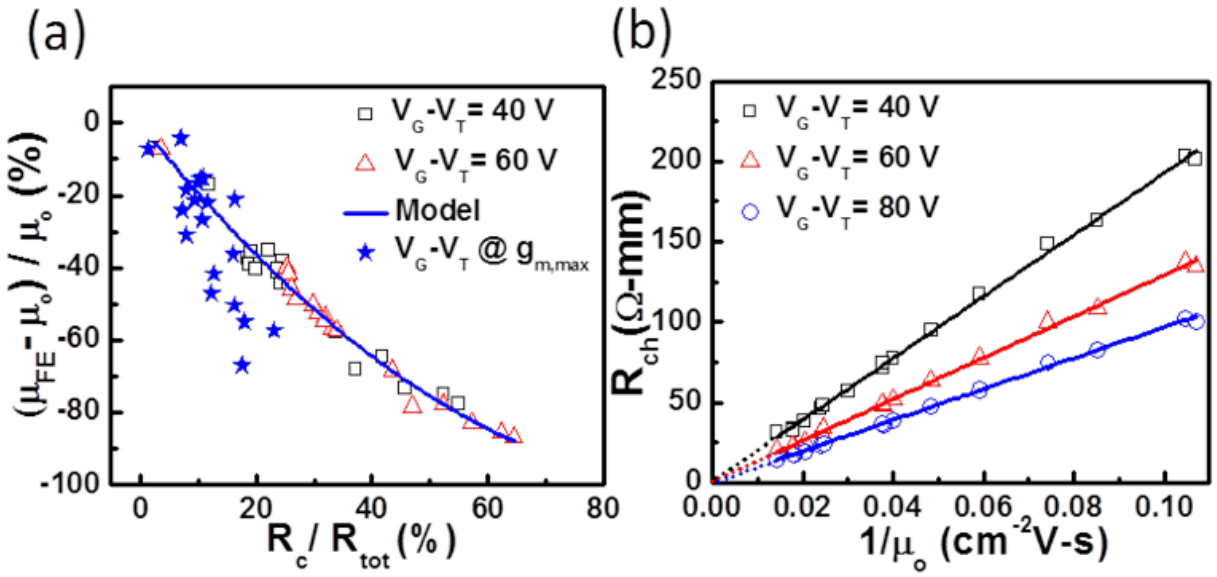

Figure 3.2. [4] Electrical data statistics from 19 MoS_2 devices highlighting the mobility underestimation error from the g_m method compared to the Y-function method. (a) Relation between the mobility underestimation extracted from g_m (μ_{FE}) compared to μ_o as a function of $R_c/R_{tot,}$. For 16 of the 19 devices, R_c/R_{tot} is in the range of 7-23 % corresponding to the mobility underestimation of 15-60 %. (b) Extracted R_c and μ_o from nineteen MoS_2 devices show that R_{ch} is directly proportional to $1/\mu_o$ as expected, and the slope is also proportional to the gate overdrive, which further validates the analytical model. The lines are visual guides reflecting the expected dependency.

Y-function robust analysis for the contact resistance extraction

In order to independently corroborate the Y-function contact resistance extraction, we fabricated two test structures for transfer length method (TLM) made with 25 nm Al_2O_3 as gate

dielectric and Au as the metal contacts. Each TLM device structure consists of 1, 0.5, and 0.25 μm channel lengths. FETs with L = 0.5 μm shown in Figure 3.3a and b are selected to represent each TLM device structure. The device shown in Figure 3.3a has negligible Schottky-barrier at room temperature as indicated by the linear response from the low-field I_D-V_D profile, while the other one shown in Figure 3.3b has an obvious Schottky-barrier. Robustness of the Y-function method is discussed and validated in the following paragraphs.

As is shown in Figure 3.3e and f, the experimental R_c data extracted from the TLM structure demonstrates a clear dependence on gate overdrive, which is in similar trend with previous published results.[46-48] In other words, the assumption of constant R_c in μ_o extraction using the Y-function method should be re-examined. According to the original equation (Equation (3)), the additional contact resistance component in the denominator does not affect the V_T extraction, i.e., the threshold voltage can still be accurately determined from the linear intercept. However, the extracted mobility ($\mu_{ext,}$) from the slope of Y in the presence of gate dependent contact resistance can in general depend on the contact resistance value (note: when R_c is constant, $\mu_{ext} = \mu_o$). One key insight from Equation (3) is that the Y-function extracted mobility can underestimate or overestimate the true low-field mobility (μ_o) depending on whether R_c' is negative or positive respectively.

The gate-dependent source and drain contact resistance is attributed primarily to the Schottky-barrier formed at the metal/MoS_2 interface.[28, 41] Electron transport across the Schottky-barrier can be well described by Fowler–Nordheim (FN) tunneling current, $I = [A^*AT^2 exp(-\Phi_B/KT)[exp(q(V_G-V_T)/nKT)-1]$,[51] where, A^* is the 2-D Richardson coefficient, A is the contact area, T is the temperature, Φ_B is the Schottky-barrier height (SBH) in unit of eV, K is Boltzmann's constant and q is the electron charge. n is the gate voltage coupling coefficient and

the metal/MoS_2 contact resistance is evaluated in the linear region rather than the sub-threshold region. For convenience, a composite fitting parameter is defined here, $a = q/nKT$. The Schottky-barrier induced metal/MoS_2 contact resistance, therefore, can be interpreted as

$$R_c = R_m + R_o exp\left[-a\left(V_G - V_T\right)\right], \tag{5}$$

where the former term (R_m), a voltage independent contribution arising from the finite metal Ohmic resistance, is the limiting series resistance under high gate overdrive; and the latter term is the gate voltage dependent term derived from the Schottky interface, where R_o is the maximum value of the Schottky contribution when V_G-V_T = 0. As is shown in Figure 3.3e and f, the gate dependence of the experimental metal/MoS_2 R_c measured via TLM method can be well fitted by the exponential model. The Schottky-barrier height, $\Phi_B = kT/q\ (ln(a/R_o) - ln(AA^*T^2))$ was extracted from the exponential fit to be ~54 meV under zero gate overdrive for the Au/MoS_2 contact, which is within the published range given by recent articles (20 meV to 120 meV).[47, 48]

With the Schottky-barrier based R_c model, the robustness of the Y-function method in the presence of gate-dependent contact resistance effect in μ_o extraction can now be analyzed. Experimentally, μ_{ext} is achieved from the linear fitting of Y-function in the large gate overdrive regime corresponding to relatively high gate overdrive. In order to analyze the impact of the V_G dependence of R_c on the linearity of the Y-function under high overdrive bias, we applied the first-order approximation of the exponential R_c equation, which yield an inverse dependence between the gate overdrive and R_c, $R_c \approx R_m + R_o/(1-a(V_G-V_T))$. This simplification makes the analysis more straightforward without impacting the validity of ensuing conclusions. Substituting the simplified R_c expression into the Y-function equation (Equation (3)), under high overdrive bias where $a(V_G-V_T) >> 1$, yields

$$Y = \frac{\sqrt{\mu_o C_{ox} V_D \frac{W}{L}}}{\sqrt{1 - \mu_o C_{ox} \frac{W}{L} \frac{R_o}{a}}} (V_G - V_T) \quad (6)$$

The influence of V_G bias in the denominator of Equation (3) is eliminated in Equation (6), therefore, this first-order approximation of R_c helps to retain the linearity of the Y-function despite the underestimation of the extracted mobility. The deviation between μ_{ext} and μ_o can be expressed as $(\mu_{ext} - \mu_o)/\mu_o = \mu_{ext} C_{ox} (W/L)(R_o/a)$, which is dependent on the value of R_o/a from the R_c fitting for a measured μ_{ext}. With the aid of numerical simulations, we observed that increasing the value of R_o/a from 0 to 10^3 merely increased the deviation to 0.1 %. Based on the fitting results in this work of the experimental data, a reasonable range for R_o/a is 10 to 100, which validates that the Y-function method is robust in μ_o and V_T extraction for realistic MoS_2 FETs.

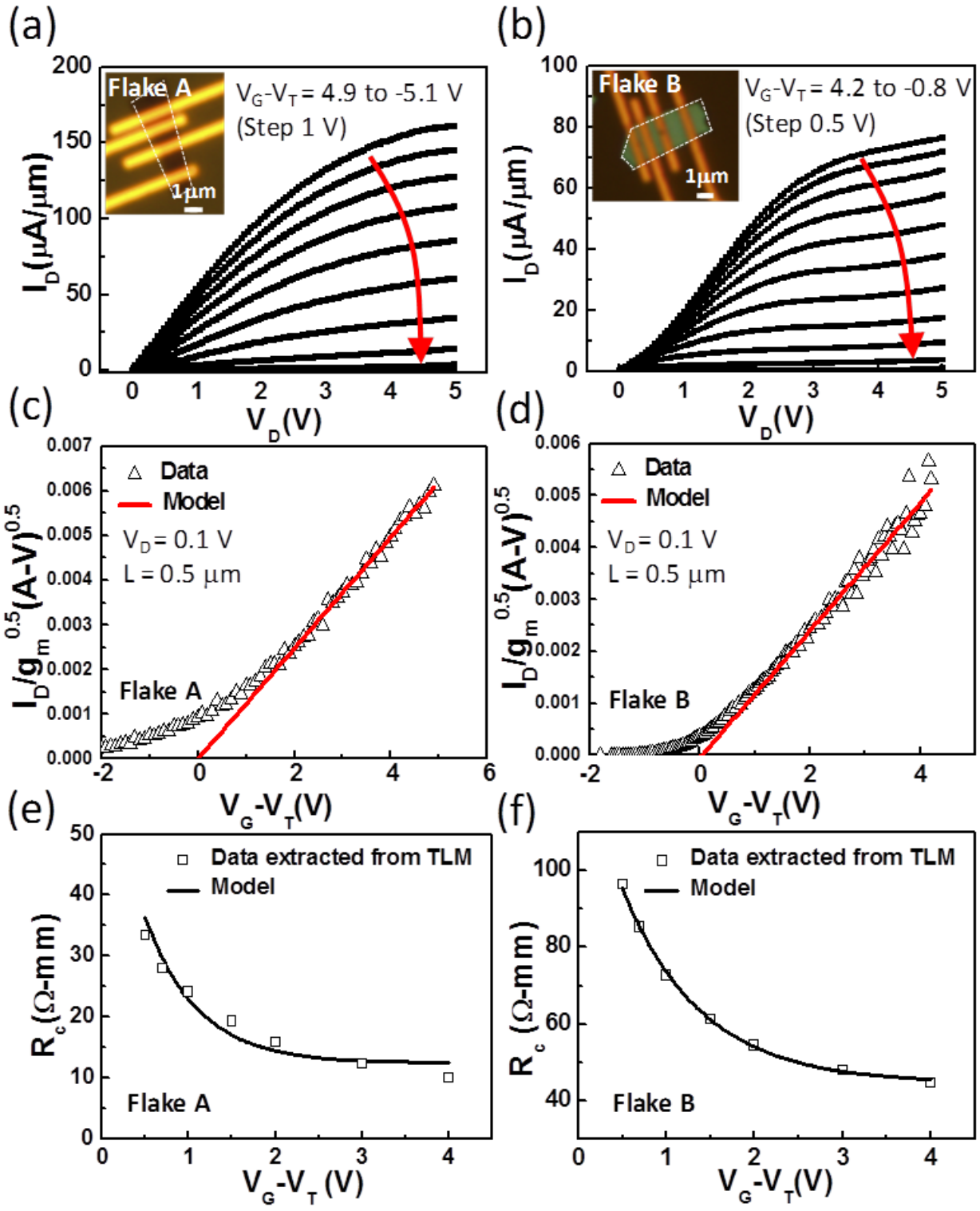

Figure 3.3. [4] (a) and (b) TLM structure made with 25 nm Al_2O_3 as the gate dielectric and Au as the metal contact. MoS_2 crystals are outlined in the optical microscope images, and the

thicknesses are 7.7 and 21.6 nm for flake A and B respectively. Each device structure includes 1, 0.5, and 0.25 μm channel lengths, and measurements are at room temperature. Devices with L = 0.5 μm are selected to represent each TLM structure. Devices made with flake A show negligible Schottky-barrier as evident by the linear low-field I_D-V_D profile, in contrast, noticeable Schottky-barrier can be seen for flake B. (c) and (d) From the linear fitting to the Y-function in the large gate overdrive region, mobility for both devices can be extracted as 29.8 and 25.1 cm^2/V-s respectively despite the presence of Schottky-barrier in the case of flake B. (e) and (f) Gate voltage dependence of R_c extracted from TLM data for flake A and flake B are presented and fitted with the exponential FN R_c model (solid line).

A comparison between contact resistance extraction methods

From the theoretical analysis shown above, we have demonstrated that the simplified Y-function method is robust for μ_o, and V_T extraction for both Ohmic contact and modest Schottky-barrier devices typical of reported TMD transistors[2, 28, 46, 48, 52]. In this paragraph, we are going to verify that extracting the contact resistance from the simplified Y-function method can be adopted as a reliable way to provide a close estimation for R_c in large gate overdrive even in the presence of Schottky-barriers. First, we examined the contact resistance by comparing the extraction from the Y-function and TLM methods (Figure 3.4), and noticed a clear discrepancy. From the assumption of $\theta \sim \mu_o C_{ox} R_c W/L$, R_c is extracted by neglecting θ_o, which results in an upper bound for R_c. However, it is shown that the R_c extracted from the Y-function is even higher than the value extracted from TLM. We examined our data more closely, and then found out that μ_o extracted from the Y-function method showed degradation with channel length from 1

m to 250 nm, and similar observation was also mentioned in a previous published result for MoS_2 bottom-gate transistors.[48, 52] This *L*-dependent mobility effect needs to be better understood and certainly considered for R_c extraction from the TLM structure. For the original extracted data, we assumed μ_o is constant over different channel lengths. Ignoring the mobility degradation introduced by channel length scaling will lead to an overestimation of R_c. Since μ_o is extracted in the large gate overdrive region, we only apply the length dependent correction to the high gate overdrive region (shaded region in Figure 3.4). With this correction, there is good agreement between R_c extracted from the Y-function method and the corrected TLM method. The overestimation of R_c extracted from the Y-function method was due to neglecting the effect of θ_o, which relates to additional mobility degradation factors such as surface roughness and remote phonon scattering.[5]

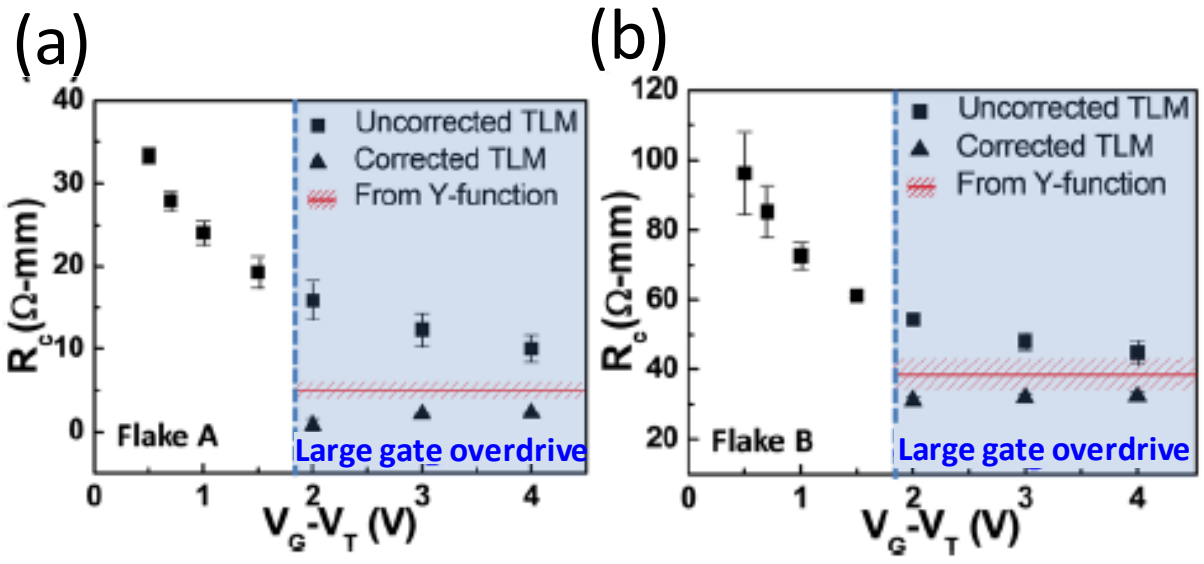

Figure 3.4. [4] (a) and (b) The same TLM structures as shown in Figure 3.3. R_c extracted from the Y-function method shows the uncertainty range for 3 different channel lengths for each TLM

structure. For flake A, the average R_c is 4.9 Ω-mm (shown as a line in Figure 3.4a), with an uncertainty range from 3.9 to 6.1 Ω-mm (shown as shaded bar), and for flake B, the average R_c is 39.6 Ω-mm (shown as a line in Figure 3.4b), with an uncertainty range from 33.6 to 44.0 Ω-mm (shown as shaded bar). With the corrected μ_o for each channel length, a good agreement between R_c extracted from the Y-function method and the corrected TLM method can be observed. The overestimation of R_c extracted from the Y-function method was due to neglecting the effect of θ_o, which relates to additional mobility degradation factors such as surface roughness and remote phonon scattering.[5]

The *L*-dependent mobility effect is studied by TLM structures on MoS_2 flakes with different thickness (Figure 3.5a). Thickness of flakes A, B, C, D are 7.7 nm, 21.6 nm, 0.8 nm, 0.8 nm respectively. In figure 3.5b, Flakes with 7.7 nm and 21.6 nm shows a reduced mobility while channel length scales down. In contrast, for the monolayer flakes, mobility shows a relatively constant along different channel length. For the L<500nm for monolayer flake, the fitting with Y-function method is not reliable enough to extract valid results, so result are not included. From comparing the *L*-dependent mobility effect on thicker flakes and monolayer, the result shows that this effect is stronger on thicker flake, suggesting that the anisotropy of MoS_2 might be the reason responsible for this effect. The out-of-plane resistance is much larger than the in-plane resistance. When device is scaled down along the length, only in-plane resistance is scaled down with the channel length, but not the out-of plane resistance, combined with that $R_{out\text{-}of\text{-}plane} >> R_{in\text{-}plane,}$ leading to the channel length dependant mobility from the Y-function extraction.

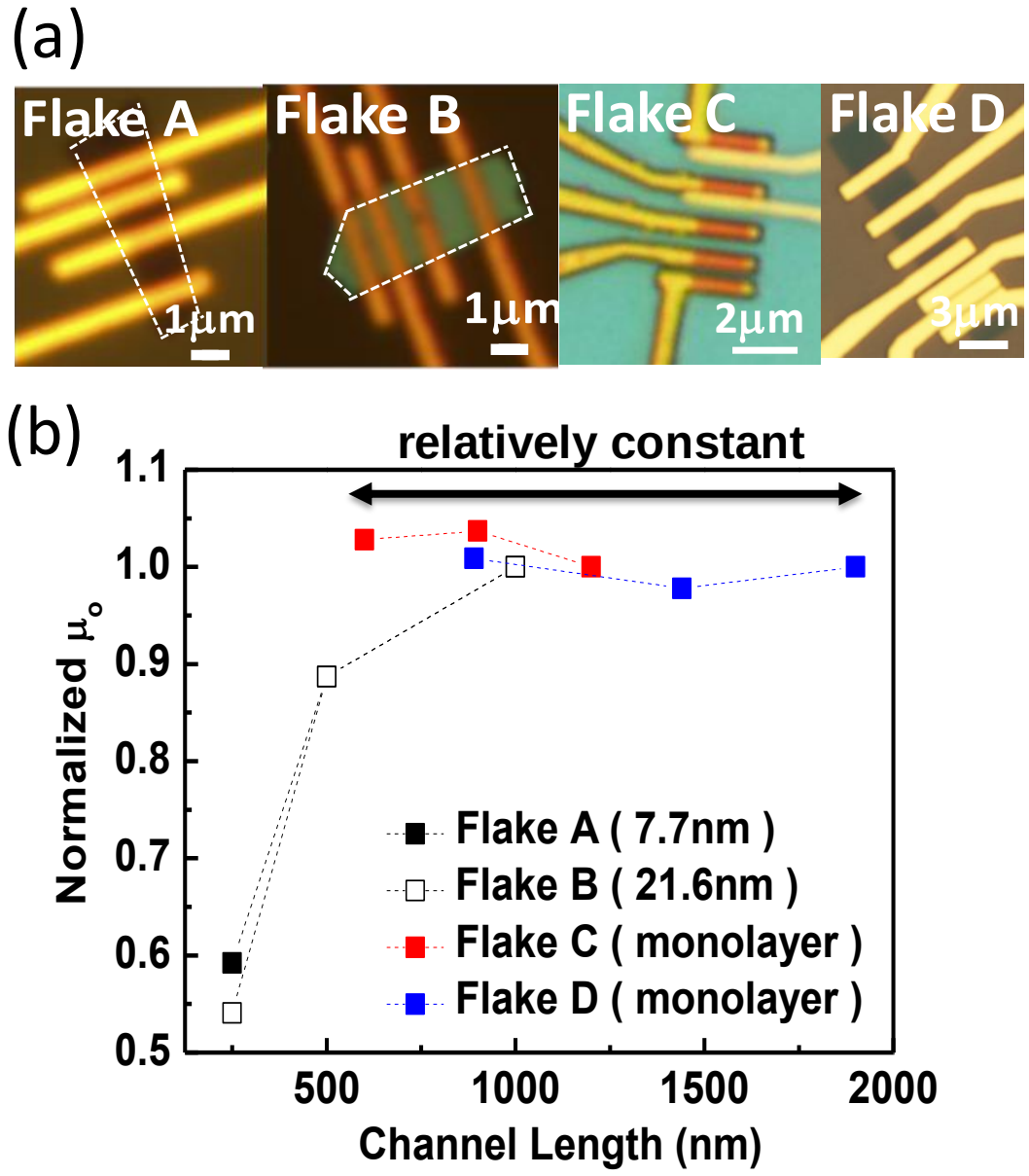

Figure 3.5. (a) Optical images of MoS_2 flakes with TLM test structures. Thickness of flakes A, B, C, D are 7.7 nm, 21.6 nm, 0.8 nm, 0.8 nm respectively. (b**)** Low field mobility versus channel length.

Conclusion

In summary, the Y-function method for FET mobility extraction has been shown to be accurate and robust in the presence of gate-dependent or Schottky-barrier contact resistance frequently encountered in semiconducting TMD transistor devices. Furthermore, independent TLM contact resistance studies corroborate the Y-function contact resistance extracted in the large gate overdrive region even for Schottky-barrier TMD FETs. By comparing the Y-function method and the corrected TLM method, we verify that the Y-function method can be adopted as a convenient way to provide a close estimation of R_c. The main conclusion of this combined experimental and analytical study is that the Y-function method is accurate for the evaluation of the low-field mobility, contact resistance, and threshold voltage for Ohmic and Schottky-barrier TMD transistor devices and is a straightforward unambiguous technique for experimental FET studies of 2D atomic sheets.

Chapter 4. Device mechanics: Failure mechanisms under strain

Failure mechanisms from bending test

To study the mechanical properties of flexible MoS_2 device, tensile strain was applied to the devices by convexly bending the flexible substrate using a home built mechanical bending fixture (Figure 4.1a). The sample was held for 10 s at each bending radius, and then released for the measurement. During the bending process, tensile strain was applied directly to the device. Owing to the sliding of the MoS_2 while bending to the smaller bending radius, the compressive strain would also be induced during the releasing process. Electrical measurements were then undertaken in order to examine the stability of several device parameters that had been subjected to the strain condition. The device parameters include mobility, ON current, and ON/OFF switching ratio. A study of the mechanical flexibility of ten devices was conducted in order to arrive at conclusions. Owing to the random orientation of MoS_2 prepared by mechanical exfoliation, the direction of the tensile strain cannot be precisely controlled. Orientation measurements of the devices indicate that they are aligned or typically within 35° of the channel length direction (the current conducting direction). The precise direction of the applied strain is not critical in this study, because the devices fail due to mechanical fatigue of the dielectric as evidenced by crack formation which we will discuss shortly afterwards. For our work and purpose, all our devices were mechanically bent until device failure was observed which allowed us to complete our mechanical modeling studies.

Figure 4.1b –d shows the dependence of the normalized mobility, normalized ON current, and ON/OFF current ratio on the bending radius respectively. Device characteristics are robust down to a bending radius of 1 mm for HfO_2 dielectric and 2 mm for Al_2O_3, which we attribute to the high deformability of MoS_2,[31] and the relatively low strain placed on the dielectric thin films. For instance, MoS_2 devices on HfO_2 retain functional properties with less than 30% mobility degradation and 10^4 ON/OFF ratio after deformation of 1 mm bending radius. At or below 2 mm bending radius, MoS_2 devices with Al_2O_3 dielectric show significant degradation owing to structural damage to the dielectric. Similar significant failure was observed for devices with HfO_2 dielectric below 1 mm bending radius, while between 2 mm and 1 mm bending radius, a gradual or soft degradation is observed.

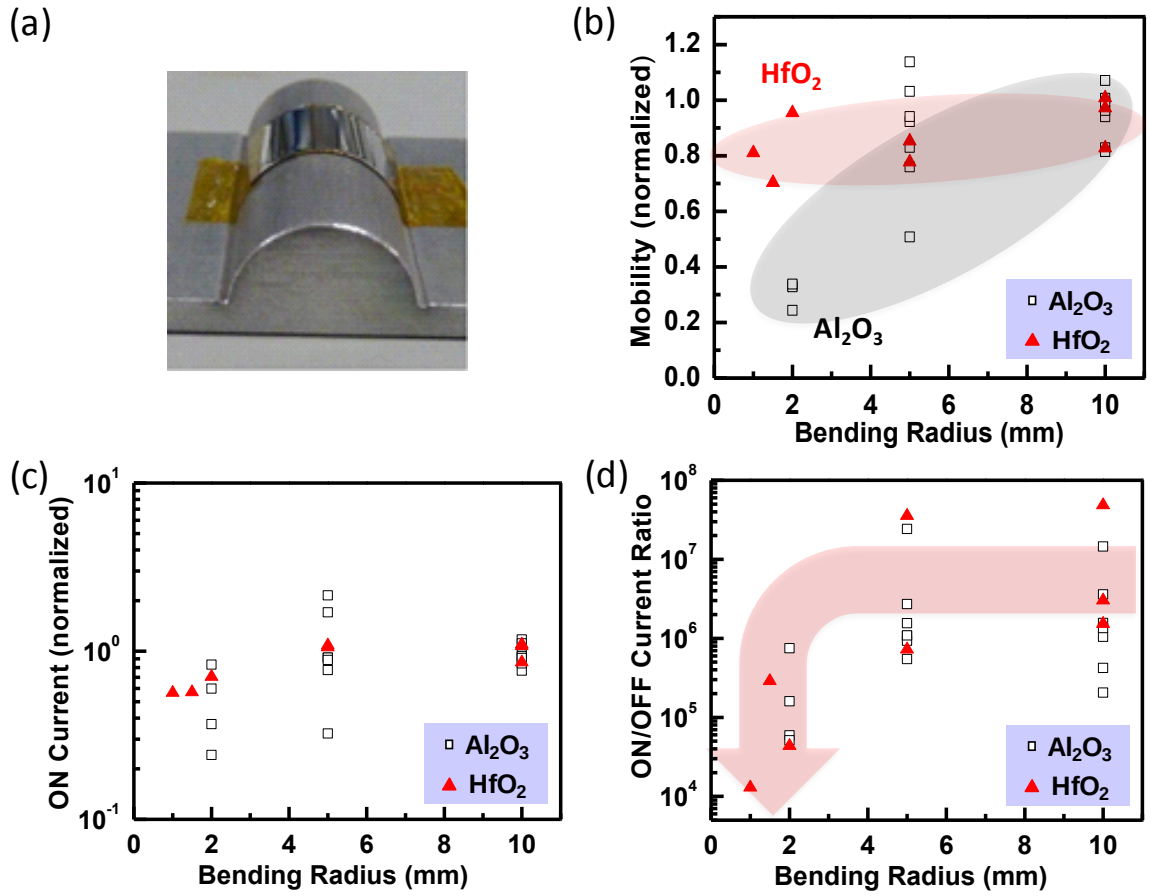

Figure 4.1. [2] A study of the mechanical flexibility of MoS_2 FETs with Al_2O_3 and HfO_2 gate dielectrics. (a) The photograph of the flexible MoS_2 sample at a bending radius of 5 mm on the experimental bending fixture. (b), (c) The dependence of the normalized low-field mobility (V_D= 0.1 V) and ON current (V_D= 1 V) on the bending radius respectively. Mechanically robust devices provide functional electrical characteristics down to a bending radius of 1 mm for HfO_2 dielectric and 2 mm for Al_2O_3 dielectric. (d) The ON/OFF current ratio (V_D= 1 V) *versus* bending radius is greater than 10^4 down to 1 mm bending radius for HfO_2 dielectric. Substantial degradation occurs below 1 mm bending radius owing to the onset of gate dielectric failure.

The Raman spectrum of the MoS_2 remains unchanged (Figure 4.2) and we confirm that the MoS_2 remains intact by AFM after the bending test, and provide several AFM images including flakes with thickness in the range of 7.9-20.1 nm which all show the MoS_2 remains intact. (Figure 4.3 and 4.4) It confirms that our devices fail due to excessive leakage current from cracks in the dielectric and not by the damage to MoS_2. From the optical microscope images, we can also observe that clear parallel cracks are formed in the dielectric in all the devices which are responsible for the failure of our devices. (Figure 4.5) One thing worth noting here is that in some occasions MoS_2 shows buckling delamination after the bending test; however, the MoS_2 maintains good mechanical contact to the electrodes and there is no evidence of crack or damage to the structural integrity. (Figure 4.6) This buckling delamination of MoS_2 decreased the gate control from the channel, causing the on current degradation shown in Figure 4.7a. Figure 4.7b shows the correlation between buckling height and thickness of MoS_2. From the equation, $G_o = \frac{\sigma_0^{\,2} t_{MoS_2}}{2\bar{E}}$ where G_o is the driving force, σ_o is the applied stress, t is thickness, and E is

Young's modulus, thicker film would have larger driving force for buckling delamination that can lead to higher buckling height.

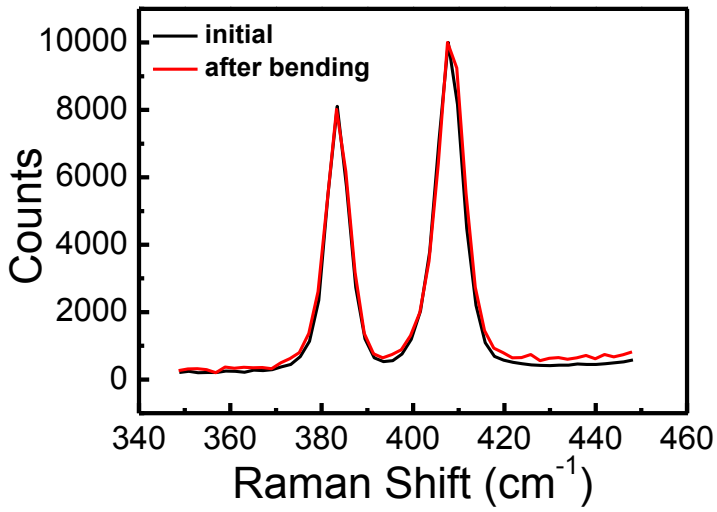

Figure 4.2. [2] The Raman spectrum of the MoS_2 remains unchanged after the bending experiment. The minimum radius used for the bending test is 1 mm.

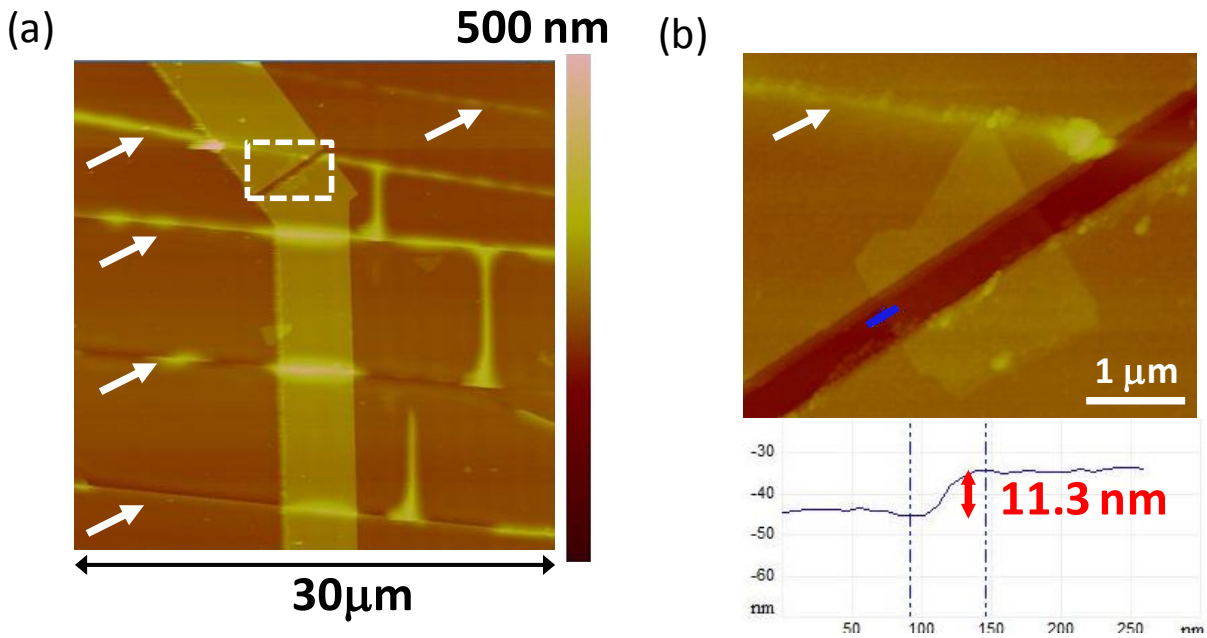

Figure 4.3. [2] (a) After bending at bending radius=0.7 mm, the AFM analysis of the MoS_2 FET shows parallel cracks (marked by arrows) formed in the HfO_2. (b) The magnification of the selected device area marked in (a) shows that MoS_2 remains intact after the bending test, confirming that our devices fail by excessive leakage current but not by damage to MoS_2. The height profile is scanned along the blue line in the top picture, showing that the thickness is 11.3 nm. This AFM analysis is in agreement with the Raman spectrum in Figure 4.2 which indicates no observable change in the MoS_2.

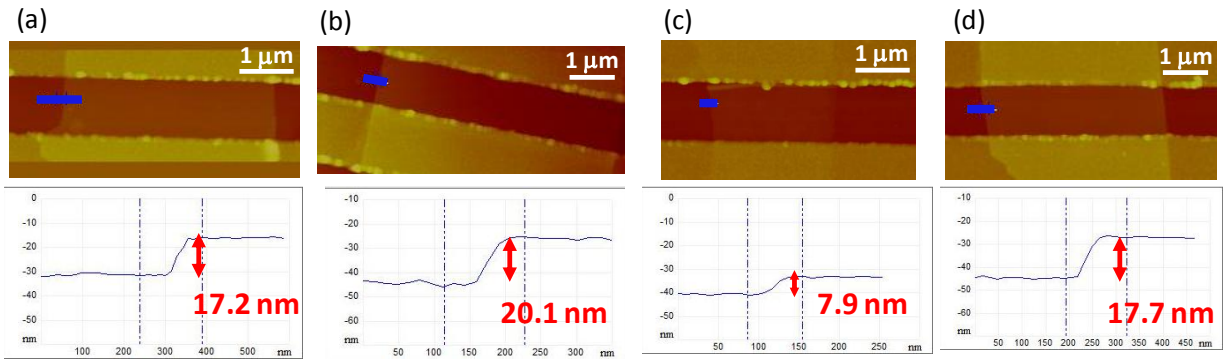

Figure 4.4. [2] (a)-(d) After bending at bending radius=2 mm, MoS_2 with various thickness ranging from 7.9-20.1 nm remains intact. The height profiles are scanned along the blue lines marked in the top pictures. No clear correlation between the thickness of flake and the bendability is found. Devices on both HfO_2 and Al_2O_3 show similar results.

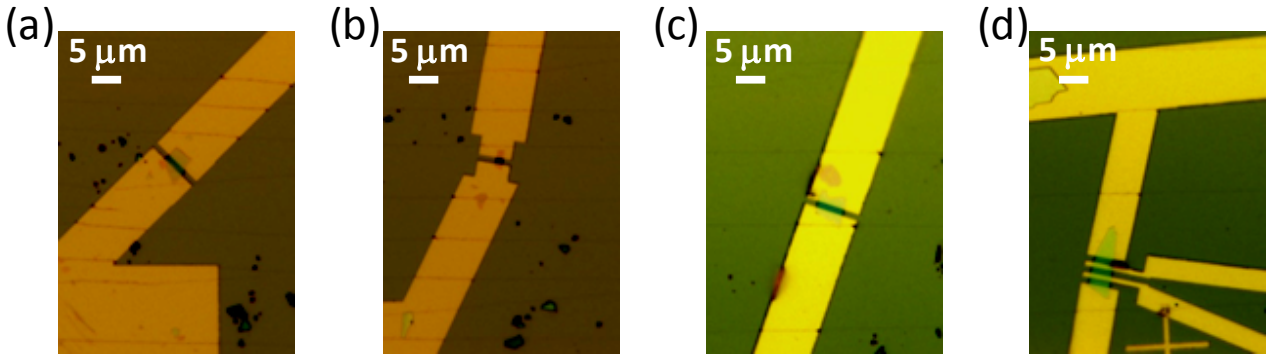

Figure 4.5. [2] From optical microscope images, we can observe that clear parallel cracks are formed in the dielectric in all the devices, which is responsible for the failure of our devices. (a) (b) Devices with Al_2O_3 as the dielectric (after bending radius=1.5 mm). (c) (d) Devices with HfO_2 as the dielectric (after bending radius=2 mm).

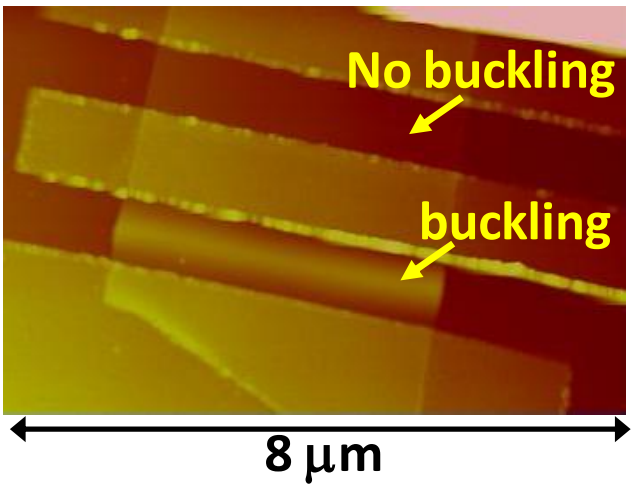

Figure 4.6. [2] In some occasions, MoS_2 shows buckling after the bending test.

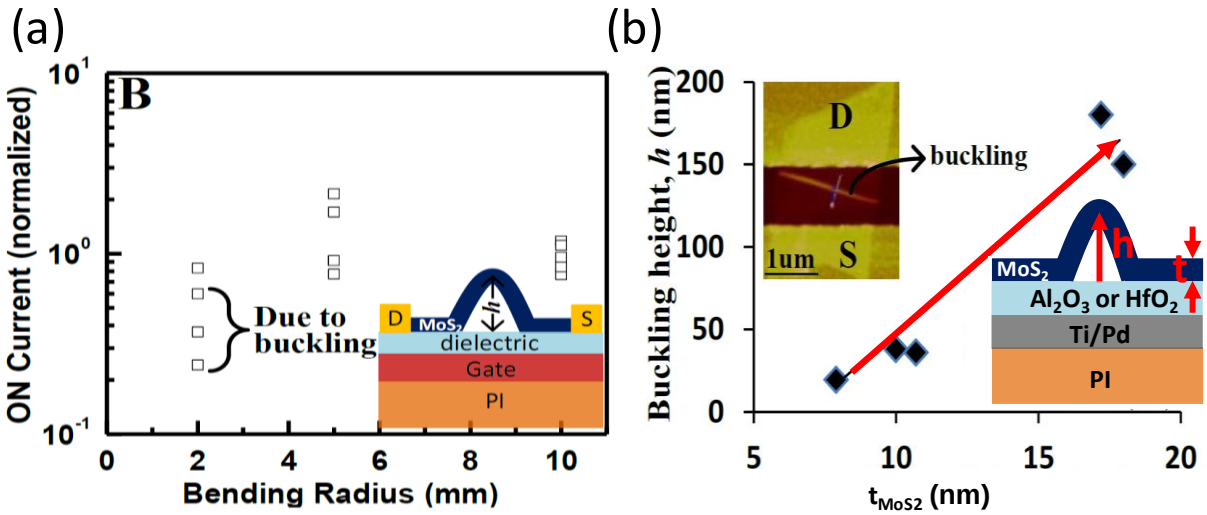

Figure 4.7. [6] (a) buckling delamination of MoS_2 after bending to 2mm. This buckling delamination decreased the gate control from the channel, causing the on current degradation. (b) Thicker film would have larger driving force for buckling delamination that can lead to higher buckling height.

Cracks in inorganic dielectrics: Stretching test

To unambiguously identify the mechanism responsible for device failure after severe bending, the gate dielectric structural integrity was investigated under varying tensile strains. For this purpose, HfO_2 and Al_2O_3 films are deposited on 26-μm-thick rectangular polyimide (PI) strips, with a sample cross-section similar to the device sample as illustrated in Figure 4.8a. Without the Kapton substrate, the thinner 26 μm PI affords a greater range of tensile strain to be studied, and maintained the same surface property as the device structure. We didn't perform our own measurements of the Young's modulus of each dielectric material but materials fabricated in very similar conditions are measured to have $E_{HfO_2} = 73.4\,\text{GPa}$, and $E_{Al_2O_3} = 163.3\,\text{GPa}$ respectively.[53]. Stretch tests were subsequently done using a home built mechanical test fixture in-situ under optical microscope (Figure 4.8b). The stretch tests revealed formation of channel cracks aligned perpendicular to the stretch direction in the dielectric materials as shown in Figure 4.8c. The growing density of dielectric cracks lead to increased gate leakage and subsequent device failure. A quantitative count of the crack density as a function of the applied tensile strain can be seen in Figure 4.8d. The critical strain and saturation crack density are extracted using an empirical model that is applicable to this work.[54] The result suggests a slightly higher critical strain for HfO_2 (1.72 %) compared to Al_2O_3 (1.69 %). We found the crack density of HfO_2 saturates at slightly higher values (~10 %) compared to that of Al_2O_3, which is consistent with the expectations that films with lower strength ($\sigma_{max} = E\varepsilon_{cr}$, where $\varepsilon_{cr}^{Al_2O_3} \approx \varepsilon_{cr}^{HfO_2}$ but $E_{Al_2O_3} > E_{HfO_2}$) exhibit lower saturation crack spacing.[55]

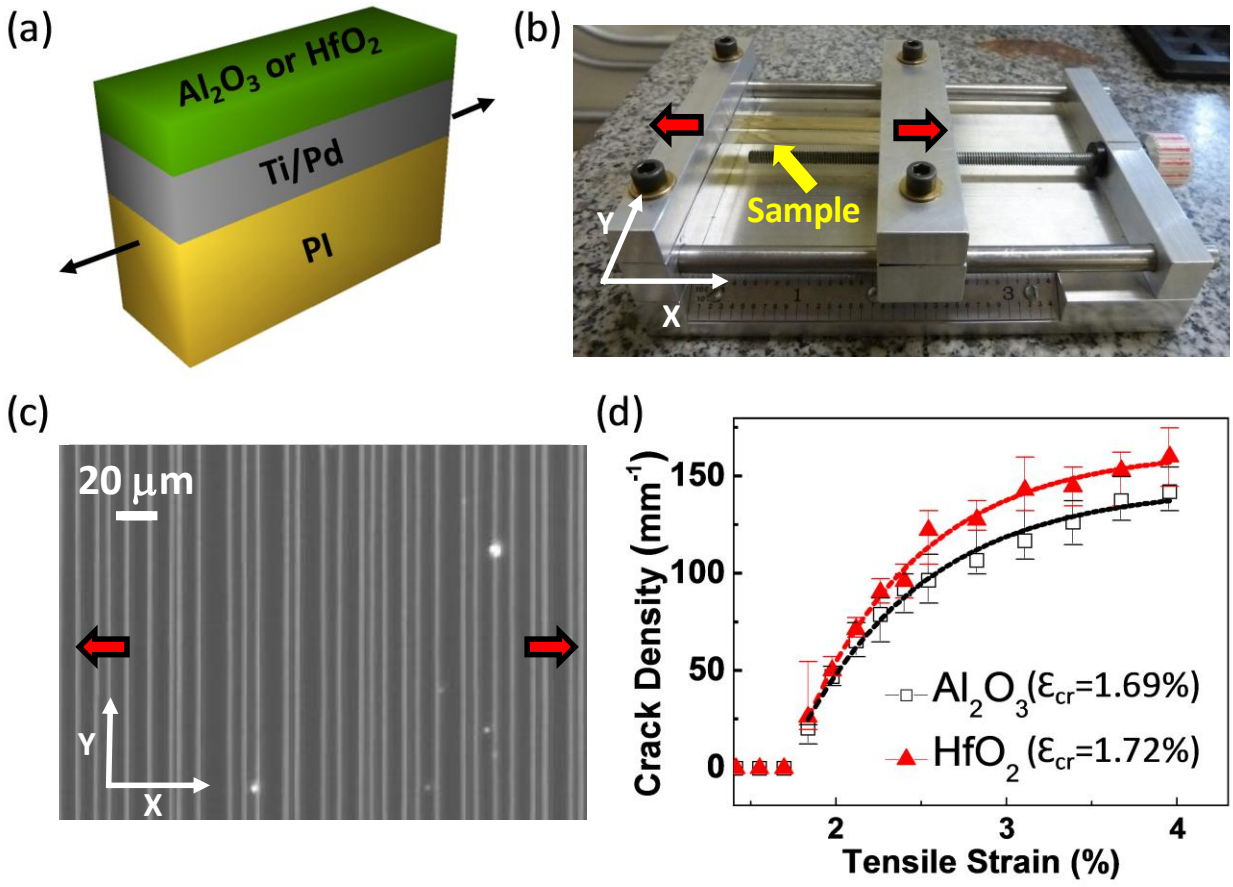

Figure 4.8. [2] (a) Test structure for the stretching experiments to elucidate the mechanical reliability of selected gate dielectrics on flexible PI. (PI 26μm /Ti 2 nm/Pd 50 nm/Al_2O_3 or HfO_2 25 nm) (b) Photograph of the stretcher test fixture. The stretching direction was along the x-direction. (c) Optical microscope image of the sample of HfO_2 at strain ~2.5 %. The parallel cracks aligned to the y-direction are due to tensile stress. (d) The dependence of the crack density on tensile strain for Al_2O_3 and HfO_2. The stretch test shows that the critical crack onset strain is around 1.69 % and 1.72 %, and the crack density saturates at 145 and 164 mm^{-1} for Al_2O_3 and HfO_2 respectively.

Time-dependent observation of the crack formation and propagation reveal that the crack propagation is substantially slower in HfO_2 compared to Al_2O_3. The measured average crack

propagation velocity is 4.9 and 28.4 μm/s for HfO_2 and Al_2O_3 respectively, which is quantitatively consistent with the exponential relation between crack growth velocity V and the energy release rate ($G \sim E\varepsilon^2$, where $\varepsilon_{cr}^{Al_2O_3} \approx \varepsilon_{cr}^{HfO_2}$ but $E_{Al_2O_3} > E_{HfO_3}$) for subcritical fracture in thin oxide films.[56, 57] This measurement suggests that HfO_2 dielectric will be more reliable under momentary deformation while the reliability under steady-state conditions is expected to be similar.

Approaches to improve device flexibility

Structures design is one of the approaches which can effectively improve the flexibility. Under pure bending, the strain, ε, at any given point in the substrate is a function of both the bending radius, ρ, and the perpendicular distance, z, from the neutral axis, given by the relationship $\varepsilon = z/\rho$. Strategies to minimize this distance include thinning the substrate or moving the device from the substrate surface to the neutral axis, for instance by two-sided encapsulation. In principle it is possible to design a highly flexible device out of a relatively brittle material, like crystalline Si.[58] For the stretch induced strain, ε is expressed as the ratio of total deformation to the initial dimension of the material body in which the forces are being applied. Similarly, by structure designs, the non-uniform stress can be enhanced to avoid the strain applied to the device region which can effectively improve the stretchability.[59]

To reveal the controlling parameters on our device bendability, we perform detailed mechanics analysis in dielectric thin films accounting for both residual strain due to thermal process during sample fabrication and mechanical strain induced by the bending test. Sample

fabrication has involved several steps of thermal process. For example, the liquid polyimide (PI-2574) is cured at 300 ºC on the Kapton substrate and the dielectric was deposited at 200 °C by ALD. Mismatch of the coefficients of thermal expansion (CTE) in the multilayers will induce residual stresses and an intrinsic curvature to the elastic multilayer stack before the bending test.

To determine the bendability of the device, *i.e.* the minimum bending radius measured from the bottom of the device before the dielectric layer starts to crack (r_{min}), we take the criterion of $\varepsilon_{tot} = \varepsilon_{cr}$ for the dielectric layer, where ε_{cr} the critical crack onset strain as is measured in Figure 4.8d. Solving this equation yields the r_{min} as a function of the thickness and Young's modulus of the substrate (t_s and E_s), as well as the thickness and Young's modulus of the dielectric layer (t_d and E_d). The result shows very weak dependence of r_{min} on t_d or E_d, but rather quite sensitive to t_s and E_s. Figure 4.9a shows the minimum bending radius, r_{min}, as a function of the substrate thickness t_s for a given substrate material, Kapton (E_s = 2.5 GPa). Since there is little effect from dielectric modulus and thickness, this curve is representative of both Al_2O_3 and HfO_2 thin films used in this paper under steady-state or long-term tensile strain. The plot reveals that decreasing the substrate thickness is an effective way to enhance the bendability of the flexible transistor. This is because decreased substrate thickness will shift the neutral axis closer to the dielectric layer. The linearity of the curve in Figure 4.9a arises from the coincidence that we are using Kapton as the substrate which has the same modulus as the liquid polyimide. If we fix the thickness of the substrate to be 76 μm and vary the substrate modulus, the minimum bending radius is shown in Figure 4.9b. It is clear that the softer substrate will offer better bendability. It is because decreased substrate modulus will also shift the neutral axis closer to the dielectric layer. As a result, the limiting bending radius of our sample could be as small as 0.45 mm if ultra-thin or ultra-soft substrates are employed. Dashed lines in both figures highlight the

conditions closest to the current experimental samples. The model predicts a minimum allowable bending radius of 2.55 mm, which is consistent with the experimental observation that gradual electrical breakdown or complete device failure are observed at a bending radius of 2 mm for both HfO_2 and Al_2O_3 dielectrics respectively.

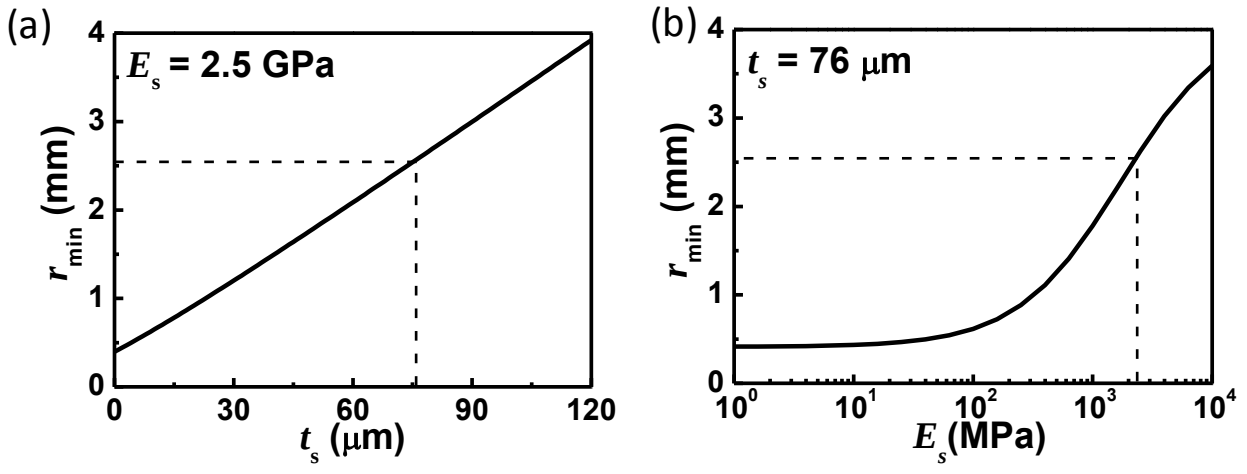

Figure 4.9. [2] (a) The predicted minimum bending radius (r_{min}) as a function of the substrate thickness with substrate modulus fixed at E_s = 2.5 GPa (Kapton). (b) The predicted minimum bending radius as a function of the substrate modulus with substrate thickness fixed at t_s = 76 μm. Curves in (a) and (b) are representative of both HfO_2 and Al_2O_3 films. Decreasing the substrate thickness or modulus can enhance the bendability of the flexible device. The dashed lines in the figures represent the conditions closest to the current experimental samples.

Besides the structure design, the other approach remained is to increase the strain limit of all the components in the device. The failure mechanisms under strain have been discussed previously. The critical strain of high-k dielectric is around 2%. As shown in Figure 4.10, by replacing the conventional high-k dielectric with the nanoscale polymer dielectric, and covering

the surface to avoid sliding between the interfaces which may result to buckling delamination, it will enable us to study the strain effect beyond 2%.

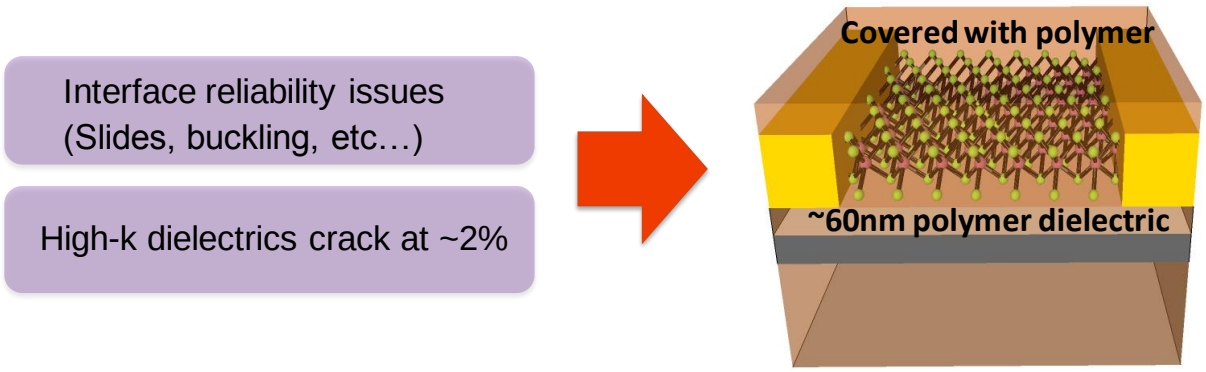

Figure 4.10. Replacing the conventional high-k dielectric with the polymer dielectric to prevent the cracks in dielectric, and covering the surface with polymer to avoid buckling delamination of MoS_2.

Solution based NPI was obtained through chemical dilution of liquid polyimide (LPI) precursor (HD MicroSystems) with N-Methyl-2-pyrrolidone (NMP) (Sigma-Aldrich), followed by the curing process at 250 ℃ under nitrogen atmosphere for 2 hours. The thickness of NPI can be controlled by the speed of spin-coating as well as various viscosities obtained by different volume ratio mixing of LPI and NMP. Figure 4.11a shows the carbonyl region of the FTIR spectrum of polyimide. Similar to the 15 μm PI on the Kapton film, 60 nm NPI on glass shows the same characteristic vibration bands near 1778 and 1720 cm^{-1}. The result is consistent with our expectation since the diluting process is not expected to change the composition of polyimide.[1] The optical transparency of 60 nm NPI is shown in Figure 4.11b. By reducing the thickness of polyimide from 15 μm to 60 nm, the transparency has improved from almost 0 to

more than 84 % for the wavelength region below 400 nm indicating that NPI is suitable for the applications on transparent substrate.

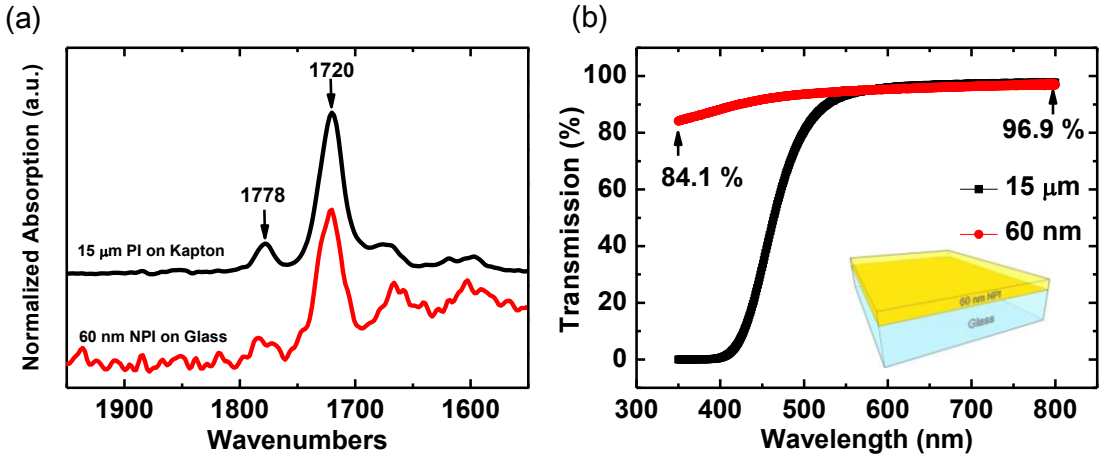

Figure 4.11. Optical studies of nanoscale polyimide. (a) Carbonyl region of the FTIR spectrum of 60 nm NPI on glass and 15 μm-thick spin-coated and cured PI on thick Kapton film. Both showed the same characteristic vibration bands near 1778 and 1720 cm^{-1}. (b) Optical transparency for PI with thickness of 60 nm and 15 μm on glass substrates. The transparency has improved from almost 0 to more than 80% for the wavelength region below 400 nm for the 60 nm-thin NPI.

Dielectric constant extracted from metal/NPI/Si with varying thicknesses is 4.08. In-situ bending measurement of metal-insulator-metal (MIM) structure on polyimide (PI) film demonstrates that NPI still remains functional under 10 % tensile-strain conditions. We employed highly doped Si substrate as the back gate, and spin coated 60 nm NPI as the gate dielectric. The channel material, MoS_2, was prepared by mechanical exfoliation of commercial crystals (SPI supplies). With this gate stack, the exfoliated MoS_2 flakes can yield good contrast for different thickness under optical microscope. Flakes with thickness between 5-20 nm were

selected and confirmed by atomic force microscope (AFM) imaging. Source/drain contacts were defined by electron beam lithography (EBL) and lift off of 50 nm Au. A schematic of the back-gated MoS_2 device is shown in Figure 4.12a. Devices have fixed channel length (1 μm) and varying channel width (0.5 – 3 μm), determined by the width of the exfoliated flakes.

Electrical characteristics of the MoS_2 FETs were then evaluated under ambient conditions. Representative transfer (I_D-V_G) characteristics are shown in Figure 4.12b. An of/off ratio of $>10^7$ and a subthreshold swing of ~450 mV/dec is observed which can be further improved by scaling down the dielectric thickness. Linear transport at low-fields and current saturation characteristics at high-fields are shown in Figure 4.12c. The field-effect mobility is in the range of 8~30cm^2/V-s for a variety of devices with the same channel dimension. The exfoliated MoS_2 flakes on NPI dielectrics show comparable device performance to the back-gated devices fabricated on SiO_2 and top-gated devices employing high-κ dielectric with the same device structure and fabrication process. As shown in Figure 4.12d, from the statistics of the mobility extracted from devices with different dielectrics, including SiO_2, high-κ dielectric (Al_2O_3), and NPI (this study), NPI shows comparable mobility to conventional dielectrics in Si fabrication process. It suggests that NPI is a promising candidate to replace the conventional high-k dielectrics for advanced flexible electronics. Moreover, with this structure, it will enable us to study the strain effect of flexible MoS_2 device beyond 2%.

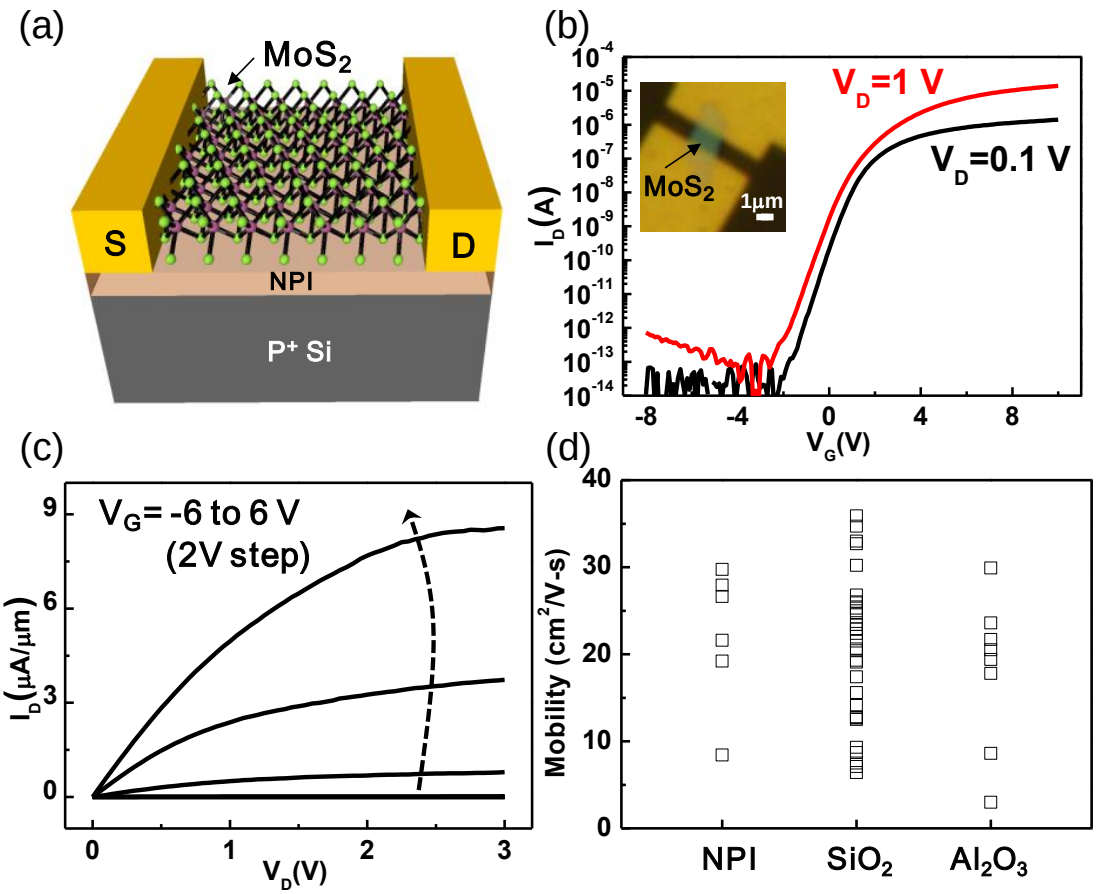

Figure 4.12. 2D semiconductor (MoS_2) TFT with nanoscale polyimide gate dielectric. (a) A schematic depiction of bottom-gate MoS_2 device. (b) Transfer characteristics of MoS_2 FETs with 60 nm of NPI dielectric. On/Off ratio is larger than 10^7. MoS_2 , which is indicated in the insert is ~12 nm-thick with channel dimensions corresponding to L=1 um and W=1.6 um. (c) Output characteristics show linear transport at low-fields and current saturation at high-fields. (d) Comparison of the field-effect mobility from several samples using NPI, SiO_2 and Al_2O_3 as gate dielectrics. NPI shows comparable mobility to conventional dielectrics in Si fabrication process.

Chapter 5. Flexible CVD MoS_2 radio frequency transistors and circuits

Growth and transfer process for MoS_2

The MoS_2 atomic layer films were grown by a standard vapor transfer growth process (schematic of growth setup shown in Figure 5.1) within a quartz tube with an inner diameter of 22 mm and a Lindberg/Blue M furnace. The starting materials were MoO_3 (15 mg) and sulfur (1 g) powder loaded in separate alumina crucibles, with the sulfur crucible outside the actual furnace and heated independently using a heating tape. The substrates used for this work were surface cleaned 285 nm SiO_2 on Si.

The procedure for the growth consisted of loading the starting material and the substrates, followed by pumping down to base pressure (< 10 mTorr), and followed by purging the tube and the gas lines by flowing in UHP N_2 gas at 200 sccm. After 4 purging cycles the tube was filled with N_2 to 1 atm pressure at flow rate of 10 sccm. Then temperature of the furnace was raised to 850 ℃ at a rate of 50 ℃/min. When the temperature of the tube furnace was at 650 ℃, the sulfur was heated to 150 ℃ (+/- 5 ℃) and held. The growth continued for 5 min at 850 ℃, and the heater to the furnace was turned off for cooling without any feedback. Heating of the sulfur was cut off once the furnace cooled down to 650 ℃.

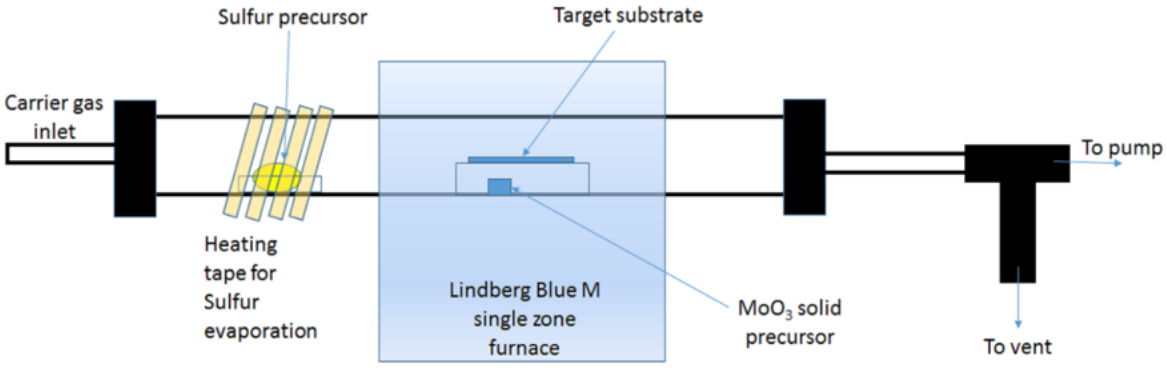

Figure 5.1. Schematic of the MoS_2 growth setup starting from MoO_3 and S.

Figure 5.2(a) shows that the CVD-grown MoS_2 is continuous over several hundreds of μm. To transfer the as–grown MoS_2 from SiO_2 to the target substrate, PMMA (A4) was spin-coated at 4000 rpm for 40 s and baked at 180℃ for 2 min. The coating and baking process was applied for four times in total. Sodium hydroxide solution (NaOH, 2M) heated at around 80℃ was used to etch away the SiO_2 under MoS_2. It enabled the PMMA-supported MoS_2 to be separated from the original substrate and be able to be transferred to the target substrate. After the transfer, the sample was stored in the desiccator overnight and baked at 180℃ for 2 min to improve the adhesion, and then soaked in aceton for 2 hours to remove PMMA. Figure 5.2(b) and (c) are the optical microscope images taken after completing the whole transfer process, showing that MoS_2 can be successfully transferred to SiO_2 and PI substrate in large area.

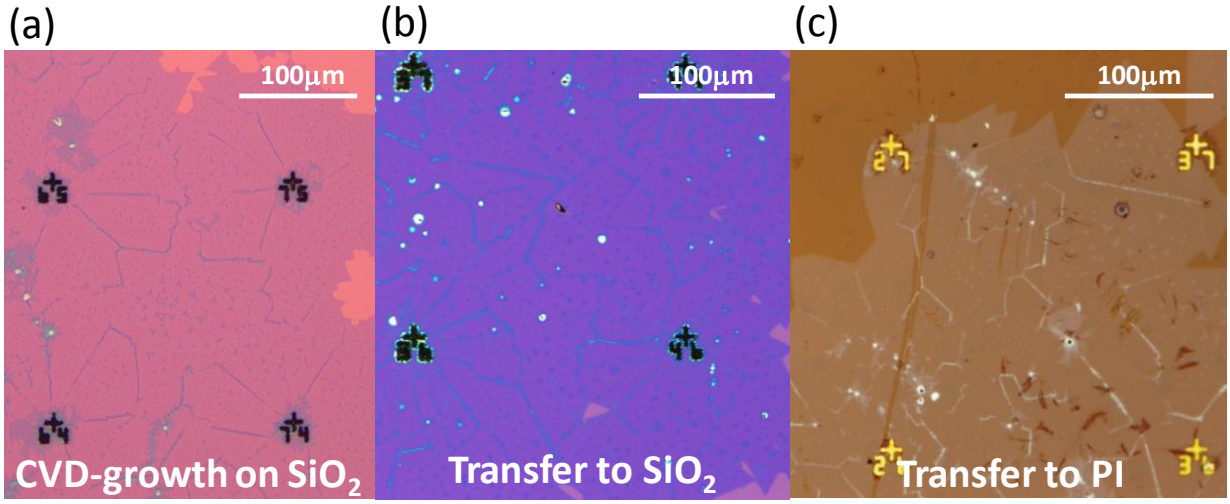

Figure 5.2. (a) Optical microscope image for the as-grown MoS_2 on Si substrate with thermally-grown 285nm SiO_2. (b) and (c) are optical microscope images of CVD-growth MoS_2 transferred to SiO_2 and PI substrate respectively.

Device fabrication and material characterization

For the device made on rigid substrate, CVD MoS_2 was transferred to 270nm SiO_2/Si as described previously. Active region was defined by electron beam lithography, followed by the dry etching process (Cl_2, 75W, 1min). Ag/Au (20/20 nm) deposited by electron beam evaporation was used as the source/drain electrode, and HfO_2 (30 nm) deposited at 200 °C by atomic layer deposition (ALD) method as the top gate dielectric. Pd (40 nm) deposited by electron beam evaporation was used as the top gate.

For the flexible devices, we used commercially available polyimide (Kapton) with a thickness of 125 μm as the flexible substrate, and spin-coated an additional liquid polyimide film (PI-2574

from HD Micro Systems) on the surface with a thickness of 13 μm to reduce the surface roughness. The liquid polyimide was cured at 300 °C for 1 hour. The same spin-coated process/cured process was repeated again on the opposite side in order to balance the residual strain induced by the curing process from the other side. HfO_2 (30 nm) was deposited at 200 °C by atomic layer deposition (ALD). The sample preparation for the flexible substrate is completed, and the remained steps are the same as the rigid sample.

Figure 5.3 shows the Raman spectra of the transferred samples compared to the as-grown samples. The peak spacing between the E^1_{2g} and A^1_g vibration mode changes from 20.4 cm^{-1} (as-grown) to 18.5 cm^{-1} (transferred). The ratio of the peak intensities also changes slightly and there is a slight widening of the peaks. As has been noted by Amani et al,[8] this change in Raman spectra can be attributed to the release of thermal strain that is inherently present in the as-grown sample. Furthermore, from the PL spectra we see a red shifting of the excitonic peak by around 45 meV and is similar to that seen by others.[60, 61] Raman and PL spectroscopy was done using a Witec Alpha 300 micro-Raman confocal microscope, with the laser operating at wavelength of 488 nm. Parameters for spectra obtained are (i) grating (Raman) = 1800 g/mm, (PL) = 600 g/mm; (ii) integration time/pixel = 1 s.

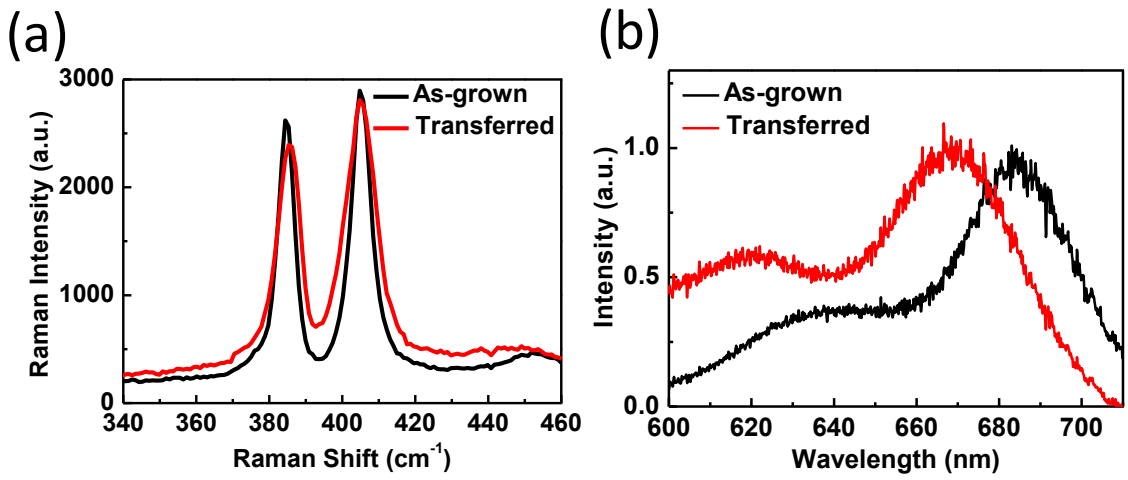

Figure 5.3. (a) Raman and (b) photoluminescence (PL) analysis for the MoS_2 before and after transfer. Both MoS_2 are on SiO_2/Si. The Raman spectroscopy shows the peak spacing between the E^1_{2g} and A^1_g vibration mode changes from 20.4 cm^{-1} (as-grown) to 18.5 cm^{-1} (transferred), which can be attributed to the release of thermal strain that is inherently present in the as-grown sample. The shift of the PL peak follows the same trend as previous reports.[60, 61]

Device studies on rigid substrates

Electrical characteristics of the transferred CVD MoS_2 FETs on SiO_2/Si were evaluated under ambient conditions. Representative transfer (I_D-V_G) characteristics are shown in Figure 5.4a. The ON/OFF switching ratio is more than 10^4. Output characteristics (I_D-V_D) as shown in Figure 5.4b shows negligible Schottky barrier in the linear region and current saturation at high fields. I_{sat} is ~250 μA/μm at V_D=5V. Using the Y-function method, the extracted low-field mobility is 53.9 cm^2/V-s (Figure 5.4c), and R_c is 2.7 Ohm-mm. Figure 5.4d verifies that the data and the model match very well. These device characteristics represent the state-of-the-art for CVD-grown

monolayer MoS_2 FETs. Table 1 summarizes the previously reported CVD-grown MoS_2 device. Our results are comparable to the best results in previous studies.[62-67]

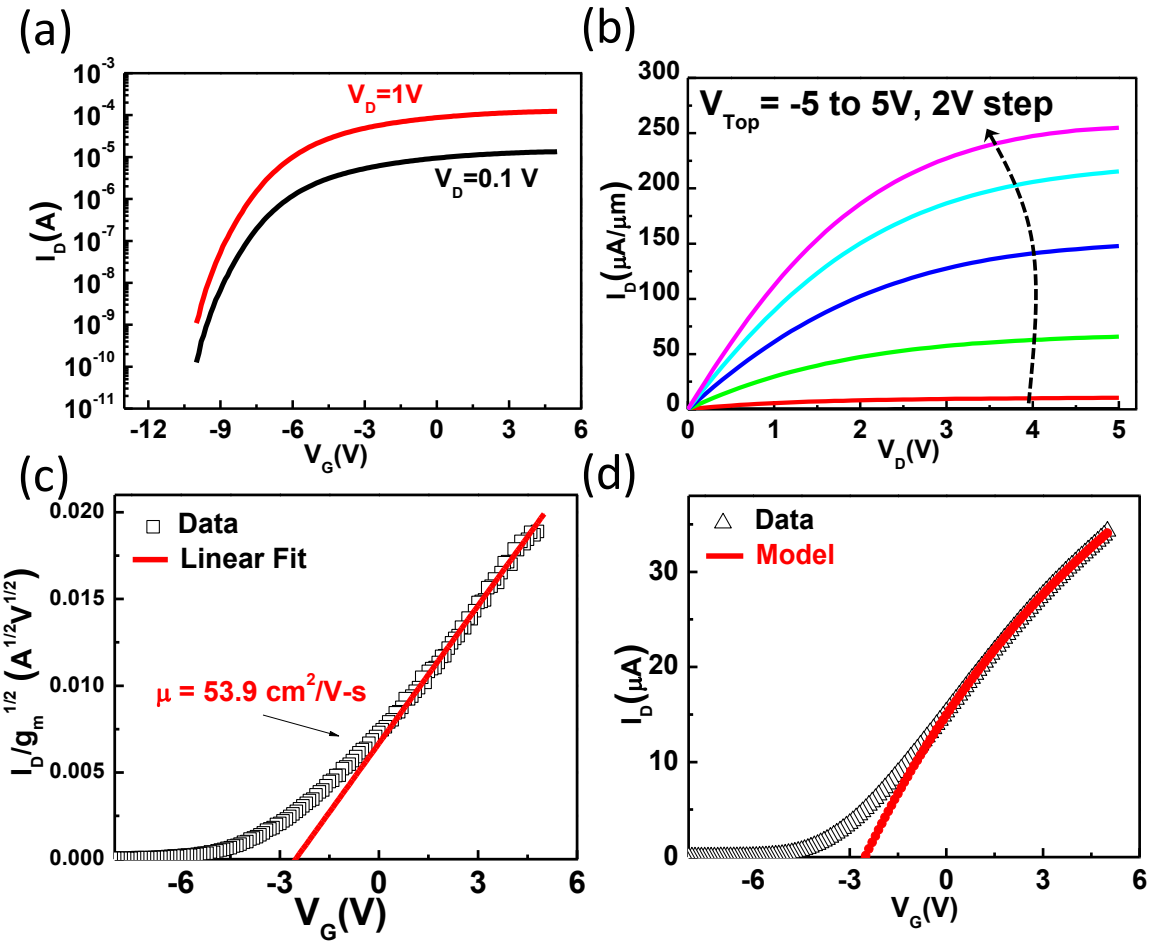

Figure 5.4. A representative MoS_2 FET (L = 1 μm) made with HfO_2 as the top-gate dielectric on flexible PI. (a) I_D-V_G characteristics in log scale. The ON/OFF current ratio is more than 4 orders of magnitude. (b) I_D-V_D characteristics in linear scale. I_{sat} is ~250 μA/μm at V_D=5V. (c) The experimental Y-function (=$I_D/\sqrt{g_m}$) profile showing the characteristic linear profile for extracting the low-field mobility. The extracted low-field mobility is 53.9 cm^2/V-s. (d) Experimental data match with the model well.

Table 1 Summary of the mobility of monolayer CVD-grown MoS_2 reported in previous studies

Ref	Mobility	Gate Stack Contact materials
This work	μ=53.9 cm^2/Vs (L=1 μm)	Top gate + HfO_2 AgAu
2015 Ref [62]	μ=24 cm^2/Vs (L=300 nm)	Top gate + HfO_2 AgAu
2014 Ref [63]	μ=56 cm^2/Vs (L=2 μm)	Bottom gate + SiO_2 1T MoS_2
2014 Ref [64]	μ=17 cm^2/Vs (L=1 μm)	Bottom gate + SiO_2 Graphene
2014 Ref [65]	μ=45 cm^2/Vs (L=10 μm)	Bottom gate + SiO_2 Au
2013 Ref [66]	μ=21 cm^2/Vs (L=1 μm)	Bottom gate + SiO_2 TiAu
2012 Ref [67]	μ=40 cm^2/Vs (L=1 μm)	Top gate + HfO_2 TiAu

To further verify the effect of the wet transfer used in our process. The transfer (I_D-V_G) characteristics of the devices with and without the transfer of MoS_2 are compared in the linear scale as shown in Figure 5.5 (Both devices are made with exactly the same device structure). The result suggests that the wet transfer used in our process does not degrade the performance.

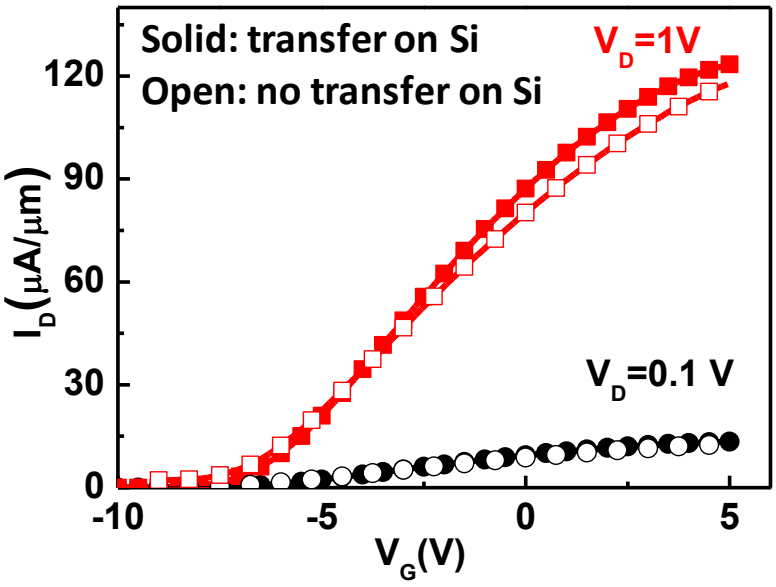

Figure 5.5. I_D-V_G characteristics are shown in linear scale. A comparison between the as-grown CVD MoS_2 FET and the transferred sample (L = 1 μm) on SiO_2/Si. Devices are with exactly the same top-gate structure.

Device studies on flexible substrates

After verifying the fabrication process on rigid substrate, similar process was applied on flexible substrate. Electrical characteristics of the transferred CVD MoS_2 FETs on flexible substrate were evaluated under ambient conditions. For applications in RF electronics, especially for high-frequency digital circuit, it is important to reduce the parasitic capacitance for the device operating in high frequency. As the result, underlap device is more favorable to reduce the parasitic capacitance especially the capacitance between gate and source/drain. However, due to the loss of the gate modulation in the gap region, it may lead to high contact resistance causing the degradation of the device performance. In order to clarify the effect of the underlap structure,

both overlap (L=500 nm with 200nm for the overlap region at each side) and underlap (L=500 nm with 125 nm gap at each side) devices were made. Optical microscope images for underlap and overlap devices are shown in Figure 5.6b and c respectively. As shown in Figure 5.6a, the transfer (I_D-V_G) characteristics in linear scale show the comparison between the underlap and overlap devices. From the analysis by using Y-function method, the low-field mobility is 21.8 cm^2/V-s (overlap) and 22.4 cm^2/V-s (underlap), and contact resistance is 4.6 (overlap) and 9.4 Ohm-mm (underlap). The ungated region at each side roughly doubles the contact resistance.

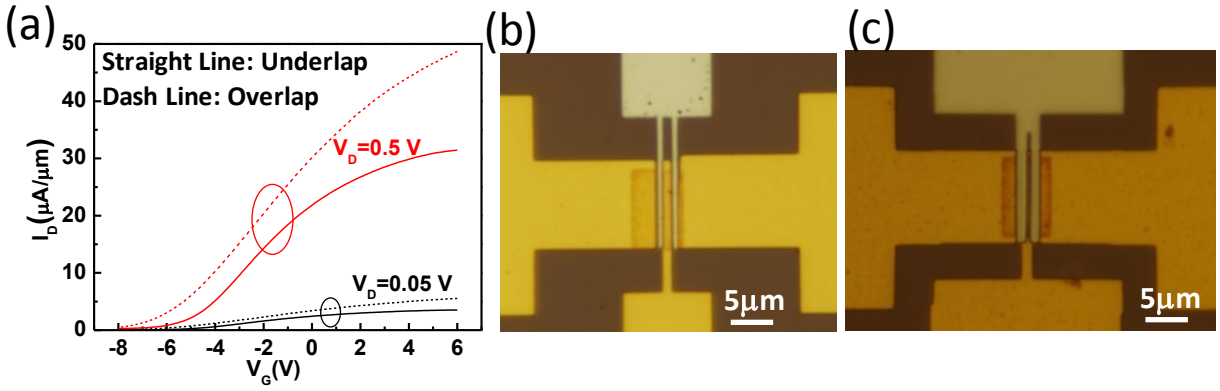

Figure 5.6. (a) I_D-V_G characteristics in linnear scale. From the analysis by using Y-function method, the low-field mobility is 21.8 cm^2/V-s (overlap) and 22.4 cm^2/V-s (underlap), and contact resistance is 4.6 (overlap) and 9.4 Ohm-mm (underlap). (b) and (c) Optical microscope image for underlap and overlap device respectively.

Figure 5.7 shows the I_D-V_G and I_D-V_D characteristics of the transferred CVD-grown MoS_2 FETs (underlap device, L=500 nm) on flexible substrate. I_D-V_D characteristics indicates negligible Schottky barrier in the linear region, and current saturation at high fields. Drain current achieves ~85 μA/μm at V_D =1.8V.

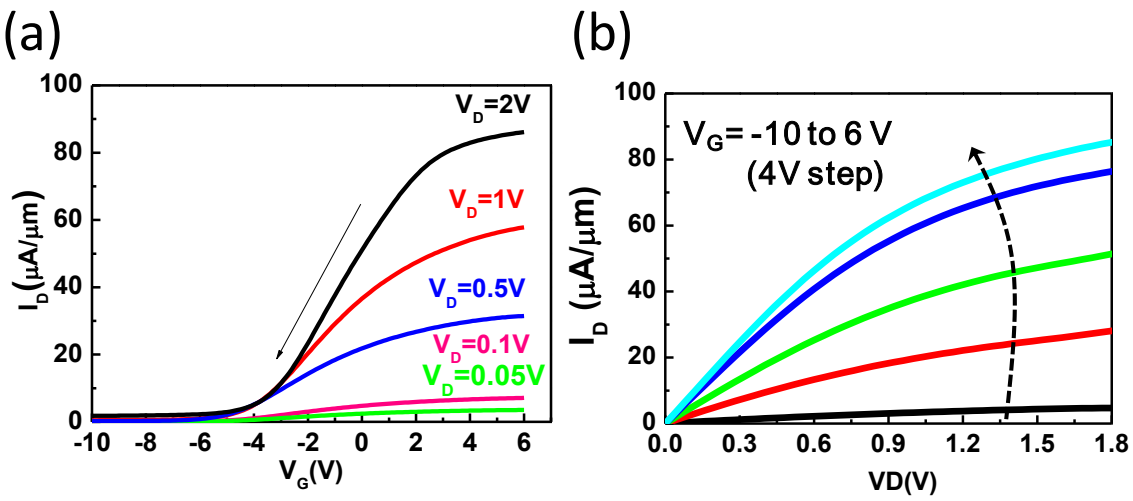

Figure 5.7. Electrical characteristics of the transferred CVD-grown MoS_2 FETs (underlap device, L=500 nm) on flexible substrate. (a) I_D-V_G characteristics in linear scale. Drain current achieves ~85 μA/μm at V_D=1.8 V. (b) I_D-V_D characteristics indicates negligible Schottky barrier in the linear region, and current saturation at high fields.

Multicycle three-point bending results was used to show the robustness of our flexible MoS_2 device. As shown in Figure 5.8a, RSA-G2 Dynamic Mechanical Analyzer (DMA) with 3-point bending fixture is used for repeated bending up to 10000 cycles. The devices were at the center of curvature of the substrate for the bending experiments. A tensile strain of 1 % was applied during the multicycle bending test. As shown in Figure 5.8b, the transfer characteristics of the flexible MoS_2 transistors demonstrate strong stability even after 10000 cycles of bending.

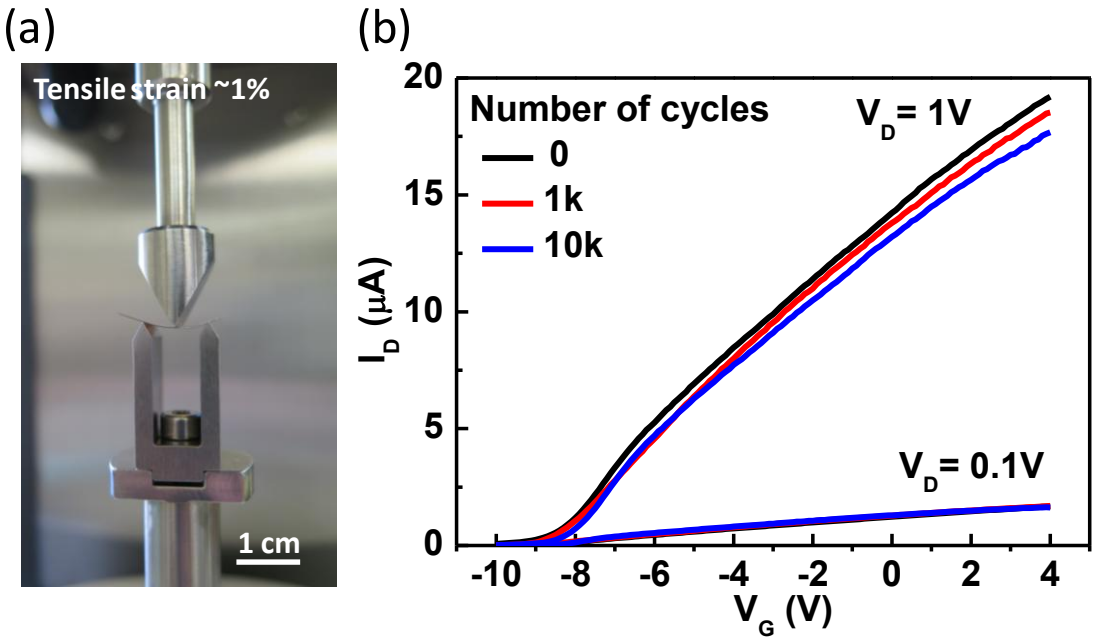

Figure 5.8. (a) RSA-G2 Dynamic Mechanical Analyzer (DMA) with 3-point bending fixture is used for repeated bending up to 10000 cycles. A tensile strain of 1 % was applied during the multicycle bending test. (b) the transfer characteristics of the flexible MoS_2 transistors demonstrate strong stability even after 10000 cycles of bending.

Flexible radio frequency transistors and amplifiers

RF measurement

The radio frequency performance of flexible MoS_2 transistor can be evaluated from the transit frequency (f_T), which is the frequency at 0dB current gain. In order to measure the transit frequency, an Agilent Microwave Network Analyzer (VNA-E8361C) was used for RF characterization in the range of 100 MHz to 10 GHz. Standard OPEN and SHORT structures (Figure 5.9) were used to de-embed parasitic capacitances and resistances to determine the intrinsic frequency performance.

The same underlap device (L_g = 500 nm) presented for DC characteristics in Figure 5.7 was used for the extraction of S-parameters. The short circuit current gain $|h_{21}|$ vs. frequency is shown in Figure 5.10a. The extrinsic f_T is measured to be 2.7 GHz while operating at the maximum g_m point (V_{gs} = -1V and V_{ds} = 2V). After applying de-embedding parameters, the intrinsic f_T reaches 5.6 GHz. The device shows good linearity in the log-scale with the expected -20 dB/dec slope.

Analytically, $f_T=v_{sat}/2\pi L$ under high-field for maximum transport. In this regime, the $f_T \cdot L_g$ and v_{sat} are the relevant performance metrics are useful metrics for device performance benchmarking. The radio frequency performance of our device corresponds to $f_T \cdot L_g$ of ~2.8 GHz-µm, and v_{sat} of $\approx 1.8\times10^6$ cm/s. As reported in other studies, the conditions of both monolayer and flexible substrate usually further degrade the performance compared to the device made with multi-layer MoS_2 on rigid substrate. However, our MoS_2 RF TFTs afford $f_T \cdot L_g$ (v_{sat}) of 2.8 GHz·um ($1.8x10^6$ cm/s), higher than previous exfoliated flexible MoS_2 and other inorganic TFTs (Figure 5.11).

Another figure of merit for high-frequency transistors is the maximum frequency of oscillation, f_{max}. This is the frequency limit at which power gain given matched input and output impedances. The maximum available gain (MAG) was obtained from the measured S-parameters as shown in Figure 5.10c. Operating at the same DC bias point, an extrinsic f_{max} of 2.1 GHz was measured. Using the same de-embedding procedure, the intrinsic maximum oscillation frequency is extracted to be f_{max} = 3.3 GHz.

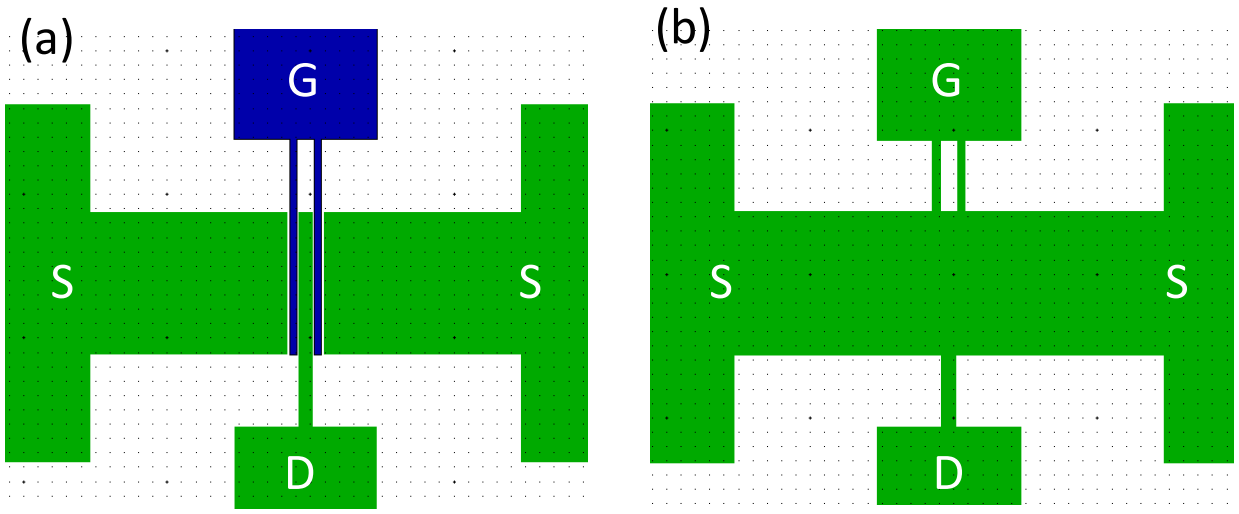

Figure 5.9. Mask design for (a) open structure, and (b) short structure.

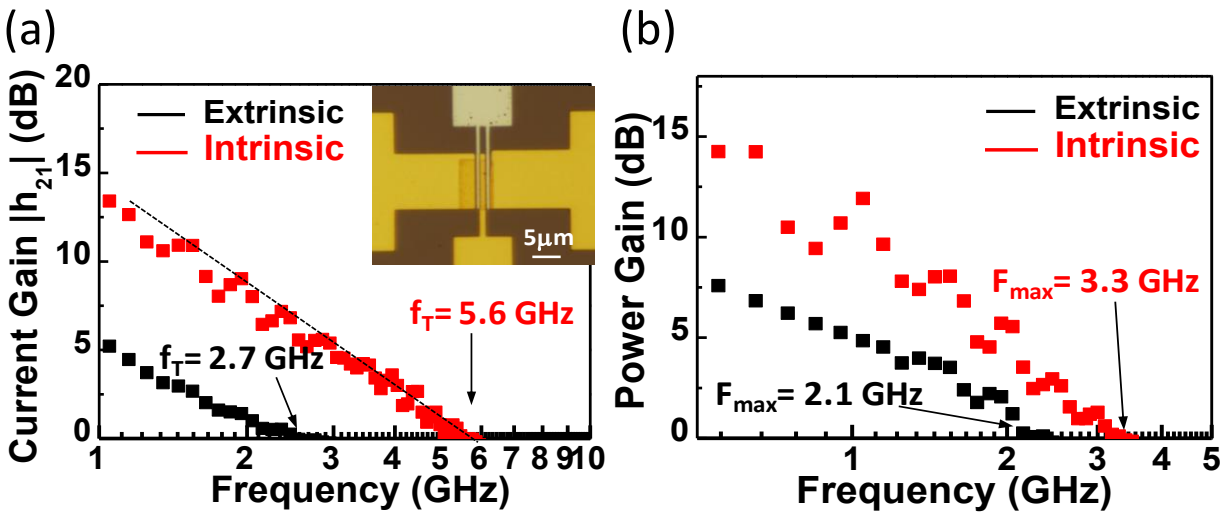

Figure 5.10. Frequency performance of MoS_2 flexible RF TFTs on PI. (a) Intrinsic f_T~5.6 GHz and fmax~3.3 GHz were achieved. L=0.5 μm, W=18 μm. The gate bias is at peak gm and V_D=2 V. Insert is optical image of RF TFT. Line is 20 dB/dec visual guide. (b) The maximum frequency of oscillation vs. frequency. Operating at the same DC bias point, an extrinsic f_{max} of 2.1 GHz and an intrinsic f_{max} of 3.3 GHz were measured.

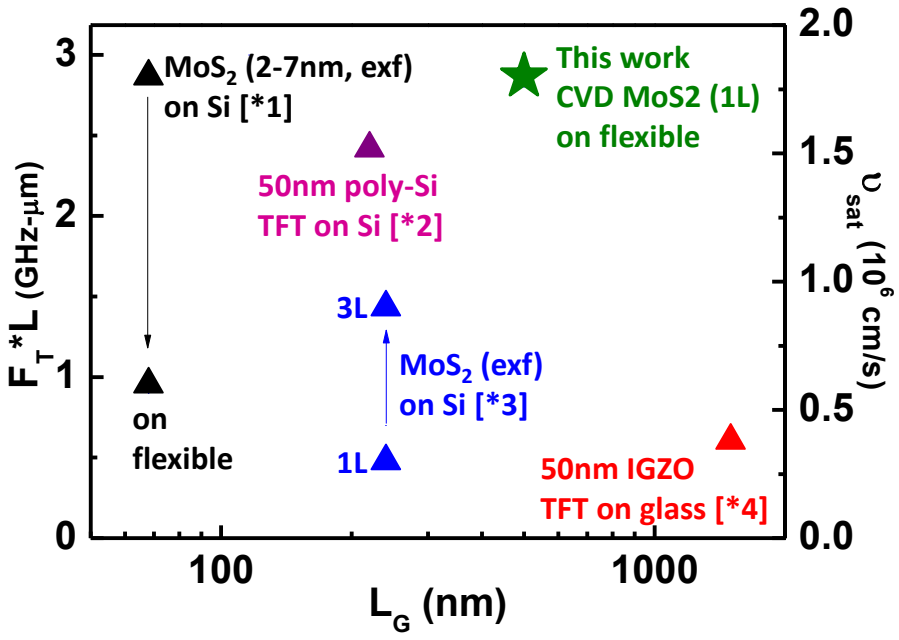

Figure 5.11. TMD RF device comparison. Benchmarking to prior results and similar TFTs (<100nm) (IGZO poly-Si) indicates our $f_T \cdot L_g$ and vsat are the highest on flexible substrates and similar to the best exfoliated MoS2 values on Si. Data from [*1] Jiang et al, Nat Comm, 2014. [*2] Chen et al, EDL, 2013. [*3] Krasnozhon et al, Nano letters, 2014. [*4] Su et al, SSE, 2015.

Amplifier

The schematic of the common source (CS) amplifier is shown in Figure 5.12a. An RF input (V_{in}) is applied to the gate terminal of the FET and the drain output (V_{out}) is connected to an oscilloscope (1 MΩ load). Bias tees were used for routing the DC bias and AC signals. The MoS_2 FET is biased at the same maximum transconductance point (V_{gs} = -1 V, V_{ds} =2 V). Applying an input sine wave at 1.4 MHz, a voltage gain ($A_v = V_{out}/V_{in}$) of 15 dB (Figure 5.12b) was measured.

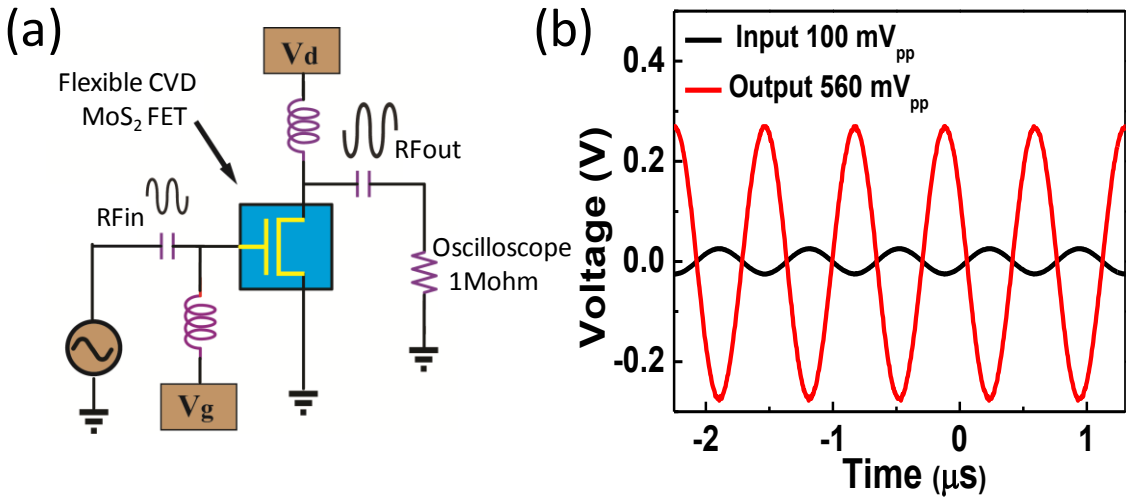

Figure 5.12. (a) The schematic of the common source (CS) amplifier. (b) Operated at the same maximum transconductance point (V_{gs} = -1 V, V_{ds} =2 V), applying an input sine wave at 1.4 MHz, a voltage gain ($A_v = V_{out}/V_{in}$) of 15 dB was measured.

Conclusion

In conclusion, flexible CVD-grown MoS_2 FETs were demonstrated to be suitable for high frequency operation. Our studies yield the highest CVD-grown MoS_2 device properties on flexible substrates to date. Intrinsic transit frequencies of 5.6 GHz and intrinsic maximum oscillation frequencies of 3.3 GHz are achieved. The radio frequency performance of our device corresponds to $f_T \cdot L_g$ of ~2.8 GHz-μm, and v_{sat} of ≈ 1.8×10^6 cm/s which are compatible to the best results made with multi-layer MoS_2 on rigid substrate. Furthermore, multicycle three-point bending results demonstrated the strong stability of our flexible MoS_2 transistors even after 10000 cycles of bending. Additionally, the common source (CS) amplifier was demonstrated, yielding a voltage gain of 15 dB for an input sine wave at 1.4 MHz. These results indicate that

MoS_2 can serve as a suitable semiconducting material for low-power, high speed devices for flexible electronics and smart systems owing to its unique combination of large bandgap, high mobility and high strength. The large-area CVD-grown MoS_2 provides a practical rout to realize high speed electronics circuit applications in the future.

Chapter 6. Conclusions

High performance and highly bendable multi-layer MoS_2 FET on the flexible substrate

We report the first comprehensive study of MoS_2 FETs using conventional solid-state high-k dielectrics on flexible substrates. Our studies yield the highest MoS_2 device properties on flexible substrates to date, with ON/OFF ratio greater than 10^7, sub-threshold slope of ~82 mV/decade, and low-field mobility of 30 cm^2/V-s. Furthermore, experimental investigation of the mechanical flexibility reveals that device characteristics are functional down to a bending radius of 1 mm for HfO_2 gate dielectric. Comparative studies of the two high-k dielectrics (Al_2O_3 and HfO_2) used in this research determine that HfO_2 affords a slower crack propagation which in addition to its higher permittivity, makes it a more attractive gate dielectric especially for momentary device deformation. These results indicate that MoS_2 is likely the most suitable semiconducting material for low-power, high speed devices for flexible electronics and smart systems owing to its unique combination of large bandgap, high mobility and high strength.

Y-function method for extracting mobility and contact resistance

Contact resistance (R_c) can substantially obscure the extracted mobility based on standard transconductance or two-point conductance measurements of field-effect devices especially for low density of states materials such as MoS_2 or similar atomic crystals. Currently, there exists a pressing need for a routine technique that can decouple mobility extraction from R_c. By combining experiments and analysis, we show that the Y-function method for FET mobility extraction is accurate and robust in the presence of gate-dependent or Schottky-barrier contact

resistance frequently encountered in semiconducting TMD transistor devices. Furthermore, independent TLM contact resistance studies corroborate the Y-function contact resistance extracted in the large gate overdrive region even for Schottky-barrier TMD FETs. By comparing the Y-function method and the corrected TLM method, we verify that the Y-function method can be adopted as a convenient way to provide a close estimation of R_c. The main conclusion of this combined experimental and analytical study is that the Y-function method is accurate for the evaluation of the low-field mobility, contact resistance, and threshold voltage for Ohmic and Schottky-barrier TMD transistor devices and is a straightforward unambiguous technique for experimental FET studies of 2D atomic sheets.

Device mechanics: Failure mechanisms under strain

Experimental investigation identifies that crack formation in the dielectric is the responsible failure mechanism demonstrating that the mechanical properties of the dielectric layer is critical for realizing flexible electronics that can accommodate high strain. Our uniaxial tensile tests have revealed that atomic-layer-deposited HfO_2 and Al_2O_3 films have very similar crack onset strain (~2 %). However, crack propagation is slower in HfO_2 dielectric compared to Al_2O_3 dielectric, suggesting a subcritical fracture mechanism in the thin oxide films. On the other hand, the buckling delamination observed in MoS_2 as well which decreases the gate control from the channel, causing the on current degradation.

Structures design is one of the approaches which can effectively improve the flexibility. We demonstrated that the bendability can be improved by reducting the thickness and Young's

modulus of the substrate. Besides the structure design, the other approach remained is to increase the strain limit of all the components in the device. We susccessfully integrade the MoS_2 device with the nanoscale polymer dielectric (NPI), and the devices show comparable mobility to conventional dielectrics in Si fabrication process. This suggests that NPI is a promising candidate to replace the conventional high-k dielectrics for advanced flexible electronics. Moreover, with this structure, it will enable us to study the strain effect of flexible MoS_2 device beyond 2 %.

Flexible CVD MoS_2 radio frequency transistors and circuits

In the last part of this study, we have demonstrated that the transferred CVD-grown MoS_2 FETs on the flexible substrate is suitable for high frequency operation. Our studies yield the highest CVD-grown MoS_2 device properties on flexible substrates to date. Intrinsic transit frequencies of 5.6 GHz and intrinsic maximum oscillation frequencies of 3.3 GHz are achieved. The radio frequency performance of our device corresponds to $f_T \cdot L_g$ of ~2.8 GHz-μm, and v_{sat} of $\approx 1.8\times10^6$ cm/s which are compatible to the best results made with multi-layered MoS_2 on a rigid substrate. Furthermore, multicycle three-point bending results demonstrated the strong stability of our flexible MoS_2 transistors even after 10000 cycles of bending. In addition, the common source (CS) amplifier was demonstrated, yielding a voltage gain of 15 dB for an input sine wave at 1.4 MHz. These results indicate that MoS_2 can serve as a suitable semiconducting material for low-power, high speed devices for flexible electronics and smart systems owing to its unique combination of large bandgap, high mobility and high strength. The large-area CVD-grown MoS_2 combined with the transfer process provides a practical rout to realize high speed electronics circuit applications on the flexible substrate in the future.

Appendix A. Mechanics analysis of strain induced by thermal process and bending test

The total strain in the dielectric layer (ε_{tot}) is a superposition of the thermal strain due to sample fabrication (ε_t) and the mechanical strain due to the bending test (ε_b). Here gives the detailed derivation of both strains. For the purpose of mechanical modeling, we have adopted the following material properties: $E_{\text{Kapton}} = 2.5\text{GPa}$, $\nu_{\text{Kapton}} = 0.34$, $\alpha_{\text{Kapton}} = 20\text{ppm/}^{\circ}\text{C}$,[68] $E_{\text{PI}} = 2.5\text{GPa}$, $\nu_{\text{PI}} = 0.34$, $\alpha_{\text{PI}} = 50\text{ppm/}^{\circ}\text{C}$,[69] $E_{\text{Pd}} = 121\text{GPa}$, $\nu_{\text{Pd}} = 0.39$, $\alpha_{\text{Pd}} = 12\text{ppm/}^{\circ}\text{C}$,[70] $E_{\text{HfO}_2} = 76\text{GPa}$, $\nu_{\text{HfO}_2} = 0.2$, $\alpha_{\text{HfO}_2} = 9.34\text{ppm/}^{\circ}\text{C}$,[53, 71] and $E_{\text{Al}_2\text{O}_3} = 167\text{GPa}$, $\nu_{\text{Al}_2\text{O}_3} = 0.21$, $\alpha_{\text{Al}_2\text{O}_3} = 8.4\text{ppm/}^{\circ}\text{C}$,[53, 72] where E is the Young's modulus, ν is the Poisson's ratio and α is the coefficients of thermal expansion (CTE).

A. Thermal strain

We use schematics in Figure A1 to derive thermal strains in elastic multilayer system. Assume each layer has different Young's modulus, thickness, CTE, and overall temperature change (Figure 4.9a). Thermal effect can be analyzed by using the overall temperature change of each layer, meaning that we only care about the difference between the initial and the final temperature of each layer and overlook any intermediate temperature changes.

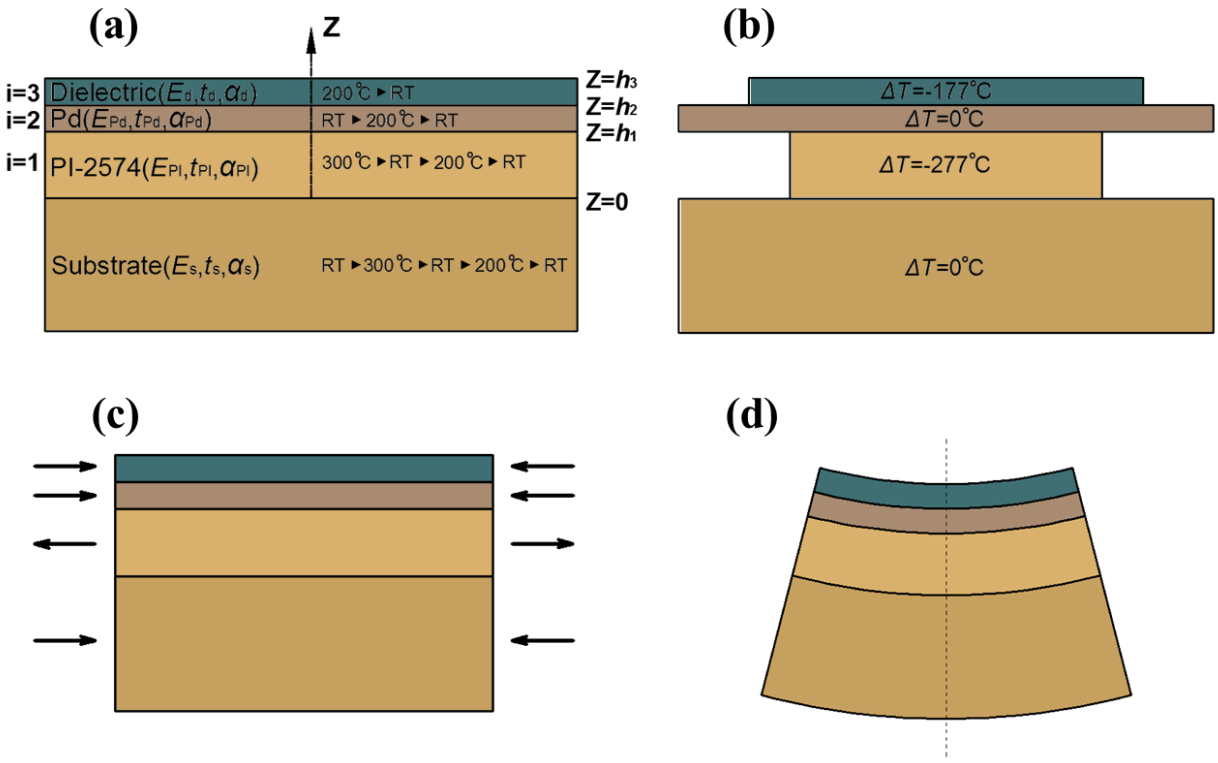

Figure A1. Schematics to calculate thermal strain. (a) The complete multilayer stack with coordinates and the temperature history of each layer. (b) Free thermal expansion of each layer assuming no constraint between layers. (c) Stresses are applied to every layer to impose displacement compatibility. (d) The ultimate configuration of the multilayer stack due to thermal effect.

Assume each layer of the system experiences an unconstrained differential temperature change, resulting differential elongation or shrinkage (Figure A1b). Then layer-wise uniform tension/compression is imposed on each of the layers to achieve a displacement compatibility, such that the strain in the system is a constant, *c*, and the net force on the system remains zero (Figure A1c). Then bending occurs due to the asymmetric stress in the layer. The total strain in the system is in the form of

$$\varepsilon = c + \frac{z - t_b}{R} \quad \text{(A1)},$$

where c is the uniform strain in each layer we imposed to achieve the displacement compatibility, R is the radius of the neutral axis, z is the distance from the top of the substrate (i.e. the bottom layer) to the position that we are interested in. The neutral axis of the whole multilayer stack is located at $z = t_b$.

Then the normal stresses in the substrate and films σ_s and σ_i are related to the total strains by

$$\sigma_s = \overline{E}_s(\varepsilon - \alpha_s \Delta T_s), \ \sigma_i = \overline{E}_i(\varepsilon - \alpha_i \Delta T_i) \quad \text{(A2)},$$

where $\overline{E}$ denotes the plane strain Young's Modulus, α is the thermal expansion coefficient and ΔT is the temperature change. The lower script s and i denote the substrate and layer i of the film, respectively.

Acknowledging the fact that, 1-the resultant force due to the uniform strain component is zero; 2-the resultant force due to the bending strain component is zero; 3-the sum of the bending moment with respect to the bending axis is zero, we are able to solve all the unknowns, which are c, t_b and r:

$$c = \frac{\overline{E}_s t_s \alpha_s \Delta T_s + \sum_{i=1}^{n} \overline{E}_i t_i \alpha_i \Delta T_i}{\overline{E}_s t_s + \sum_{i=1}^{n} \overline{E}_i t_i} \quad \text{(A3)},$$

$$t_b = \frac{-\overline{E}_s t_s^2 + \sum_{i=1}^{n} \overline{E}_i t_i (2h_{i-1} + t_i)}{2(\overline{E}_s t_s + \sum_{i=1}^{n} \overline{E}_i t_i)} \quad \text{(A4)},$$

$$\frac{1}{R}=\frac{3\left[\overline{E}_{\mathrm{s}}(c-\alpha_{\mathrm{s}}\Delta T_{\mathrm{s}})t_{\mathrm{s}}^{2}-\sum_{i-1}^{n}\overline{E}_{\mathrm{i}}t_{\mathrm{i}}(c-\alpha_{\mathrm{i}}\Delta T_{\mathrm{i}})(2h_{\mathrm{i}-1}+t_{\mathrm{i}})\right]}{\overline{E}_{\mathrm{s}}t_{\mathrm{s}}^{2}(2t_{\mathrm{s}}+3t_{\mathrm{b}})+\sum_{i=1}^{n}\overline{E}_{\mathrm{i}}t_{\mathrm{i}}\left[6h_{\mathrm{i}-1}^{2}+6h_{\mathrm{i}-1}t_{\mathrm{i}}+2t_{\mathrm{i}}^{2}-3t_{\mathrm{b}}(2h_{\mathrm{i}-1}+t_{\mathrm{i}})\right]} \quad \text{(A5)},$$

where t donates the thickness of the layer and h is the position of the top surface of the ith layer, i.e. $h_{\mathrm{i}}=\sum_{k=1}^{i}t_{\mathrm{k}}$.

Then the strain in the dielectric layer due to the normal stress can be found as

$$\varepsilon_{\mathrm{t}}=\frac{\sigma_{d}}{\overline{E}_{d}}=\varepsilon_{d}-\alpha_{\mathrm{d}}\Delta T_{\mathrm{d}}=c+\frac{z_{\mathrm{d}}-t_{\mathrm{b}}}{R}--\alpha_{\mathrm{d}}\Delta T_{\mathrm{d}} \quad \text{(A6)}.$$

It is actually the strain due to mechanical stress in as-fabricated sample but we call it ε_{t} because it originated from the thermal process during sample fabrication. Note in this analysis, we don't narrow down to the detailed sequence of the thermal process. We just care about the initial and finial status of each layer.

B. Bending strain

For trivial beam bending problem, the bending induced strain is no more than

$$\varepsilon=\frac{y}{R} \quad \text{(A7)},$$

where y is the distance from the neutral axis to the position we are interested in, and R denotes the bending radius of the neutral axis. However, Eq. A7 only holds when a beam is bent from a

flat configuration to an arc. In the current problem, the as-fabricate sample is already curved (i.e. with a finite radius of curvature), we have to derive a new formula for bending strain taking this initial curvature into consideration. We assume the layers are perfectly attached to each other and all the cross-sectional planes remain planes after bending. Figure A2 shows two cases to consider. In both cases, the bending strain by definition is given by $\varepsilon = \frac{L_2 - L_0}{L_0}$ where L's can be expressed by R's and θ's. Noting the fact that neutral axis (L_1) does not change length during bending, we can arrive the following results for Figure A2a

$$\varepsilon_{\mathrm{b}} = \frac{y(R_1 + R_2)}{R_2(R_1 - y)} \tag{A8},$$

and for Figure A2b

$$\varepsilon_{\mathrm{b}} = \frac{y(R_1 - R_2)}{R_2(R_1 + y)} \tag{A9}.$$

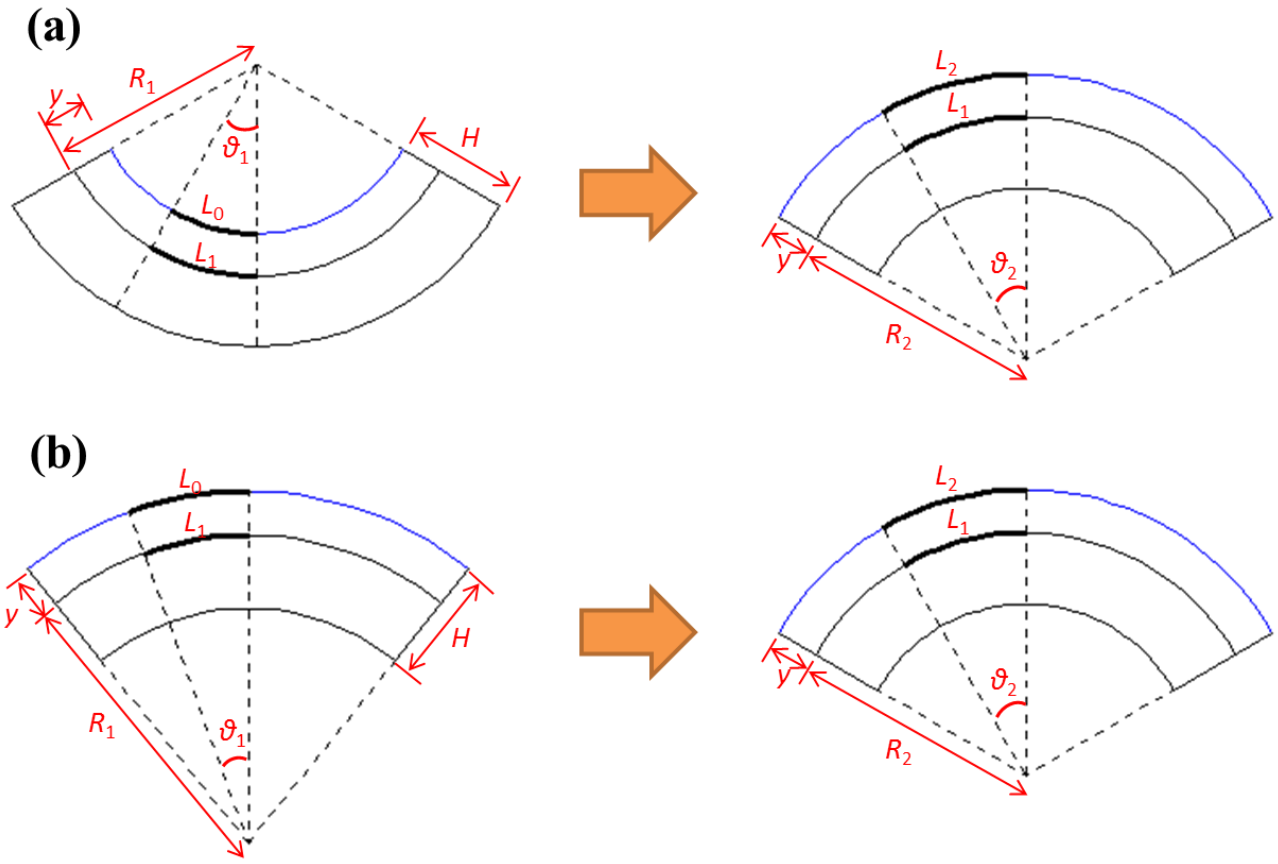

Figure A2. Schematics to help calculate the bending strain. (a) When the as-fabricated sample is bent concavely. (b) When the as-fabricated sample is bent convexly.

C. Total strain

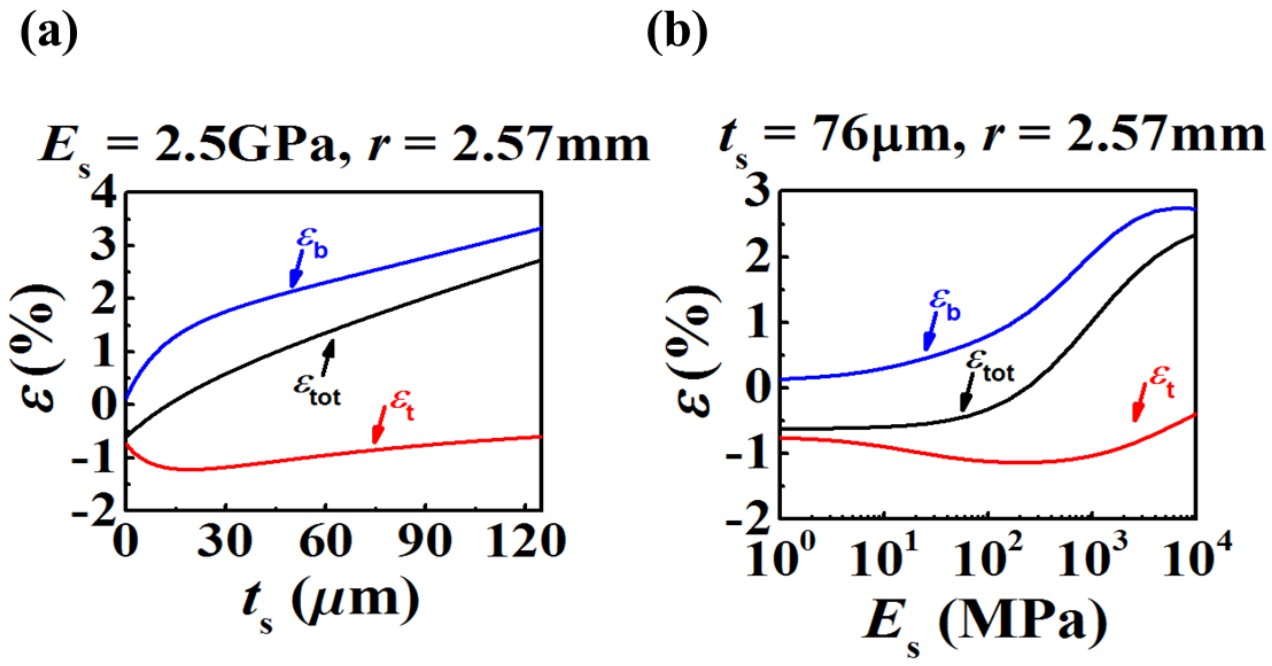

Figure A3. Thermal strain, bending strain and total strain plot as functions of substrate thickness and modulus.

Finally, the total stress-induced strain in the dielectric layer is the superposition of the thermal strain and the bending strain:

$$\varepsilon_{tot} = \varepsilon_t + \varepsilon_b \qquad \text{(A10).}$$

At a fixed bending radius of r = 2.57 mm ("r" measured from the bottom of the substrate to the origin, "R" measures from the neutral axis), the thermal strain, bending strain, and total strain are plot as functions of substrate thickness (t_s) and substrate modulus (E_s) as shown in Figure A3a and A3b, respectively. Several quick conclusions can be derived from the two plots. First, bending strain increases monotonically with t_s and E_s because larger t_s or E_s is going to induce

bigger y and hence bigger ε_b according to Eqs. A8 and A9. Second, due to the large CTE of the PI-2574 layer, the thermal strain/stress in the dielectric layer is always negative, but not monotonic with either t_s or E_s. Third, at given bending radius as small as r = 2.57 mm, although the ε_{tot} curve follows the shape of the ε_b curve pretty closely, the contribution from the thermal strain is non-trivial, and therefore cannot be neglected. Fourth, the shape of the total strain curve is monotonic, suggesting that the total strain can be reduced by reducing t_s or E_s.

The total strain is compared to the critical crack onset strain measured in Figure 4.8d to determine the minimum bending radius. Solving the following failure criterion equation

$$\varepsilon_t + \varepsilon_b = \varepsilon_{cr} \tag{A11}$$

will determine the minimum allowable bending radius, i.e. the bendability of the flexible transistor system. The results are plotted in Figure 4.9, suggesting that reducing the substrate thickness or modulus will enhance the bendability of the device. For a fixed substrate material, say Kapton (E_s = 2.5 GPa), Figure 4.9a depicts an almost linear relationship between r_{min} and t_s. This linearity is a result of numerical coincidence. As we change E_s, the shape of the curve will get distorted. Our model also predicts that when there is no substrate, i.e. t_s = 0 or E_s = 0, the minimum possible bending radius is going to approach 0.45 mm. In this case, all the functional layers are simply supported by a thin layer of PI-2574 as illustrated in Figure 2.1d.

Appendix B. Fabrication process

B1. Preparation of flexible substrate

1	DuPont™ Kapton® polyimide film (300HN for bottom gate device and 500 HN for top gate device)
2	Acetone rinse + IPA rinse + blow dry with N_2 gun
3	Attached polyimide substrates to silicon carrier wafers
4	Spin-coated liquid polyimide (PI-2574) (2000 rpm, 30 sec)
5	Soft baked at 100 °C for 10 min
6	Cured polyimide substrates in N_2 (NEYTECH furnace) - Ramp up to 200°C at rate of 4 °C/min, hold for 30 min - Ramp up to 300°C at rate of 2.5 °C /min, hold for 60 min - Cool down to 80°C at rate of -4 °C /min
7	Repeat step 4 - 6 for the other side of polyimide substrates

B2. Bottom gate MoS_2 device

1	Deposited Al_2O_3 by ALD (200 °C, 250 cycle)
2	Bottom gate - Deposited Ti 2 nm/Pd 50 nm by e-beam evaporation
3	Bottom gate dielectric - Deposited Al_2O_3 or HfO_2 by ALD (200 °C, 250 cycle)
4	Alignment mark

	- Spin-coated PMMA A4 950 (4000 rpm 40 s) - Baked at 180 °C 2 min - Spin-coated Espacer (4000 rpm 40 s) - Patterned by e-beam lithography - Rinsed with DI water for 10 s + blow dry with N_2 gun - Developed for 2 min (MIBK:IPA=1:3) + IPA rinse + blow dry with N_2 gun - Ti 2 nm/Au 40 nm or Pd 50 nm deposited by e-beam evaporation - Lift off in acetone (65 °C) + IPA rinse + blow dry with N_2 gun
5	O_2 plasma treatment by Plasmatherm 790 (O_2 10 sccm, 200 mTorr, 50 W, 1 min)
6	MoS_2 exfoliation
7	Suitable flakes selected by OM and AFM
8	S/D - Spin-coated PMMA A4 950 (4000 rpm 40 s) - Baked at 180 °C 2 min - Spin-coated Espacer (4000 rpm 40 s) - Patterned by e-beam lithography - Rinsed with DI water for 10 s + blow dry with N2 gun - Developed for 2 min (MIBK:IPA=1:3) + IPA rinse + blow dry with N_2 gun - Deposited Ti 2 nm/Au 50 nm or Au 50 nm by CHA - Lift off in acetone (65 °C) + IPA rinse + blow dry with N_2 gun
9	Measurement

B3. Wet transfer process of CVD-grown MoS_2

step	details
1	CVD-grown MoS_2 on SiO_2/Si
2	Spin coated PMMA - PMMA A4 950 (4000 rpm, 40 s) - Baked at 180 °C 2 min
3	Repeated step 2*4 times
4	Etched SiO_2 and separated MoS_2 from the original substrate - Sodium hydroxide solution (NaOH, 2M) heated at around 80℃ - Soaked the MoS_2 sample in NaOH solution for ~ 15 min - Used tweezers to separate the PMMA and the sample - Left MoS_2 floating on the surface of the solution - Used Si substrate to fish out the PMMA-supported MoS_2 and rinsed it with DI water - Finally transferred to the target substrate
5	Stored in the desiccators overnight
6	Baked at 180 °C for 2 min to improve the adhesion
7	Soaked in acetone for 2 hours to remove PMMA

B3. Top gate MoS_2 device

1	Deposited HfO_2 by ALD FIDJI (200 °C, 250 cycle)
2	Alignment mark - Spin-coated PMMA A4 950 (4000 rpm 40 s) - Baked at 180 °C 2 min

	- Spin-coated Espacer (4000 rpm 40 s) - Patterned by e-beam lithography - Rinsed with DI water for 10 s + blow dry with N2 gun - Developed for 2 min (MIBK:IPA=1:3) + IPA rinse + blow dry with N_2 gun - Deposited Ti 2 nm/Au 40 nm or Pd 50 nm) by e-beam evaporation - Lift off in acetone (65 °C) + IPA rinse + blow dry with N_2 gun
3	CVD-grown MoS_2 transfer
4	MoS_2 active region - Patterned by e-beam lithography (PMMA A4 950) - Etched by Plasmatherm 790 (Cl_2, 75W, 1 min) - PMMA removal in acetone 10 min + IPA rinse + blow dry with N_2 gun
5	S/D - Spin-coated EL6 (4000 rpm 40 s) - Baked at 180 °C 2 min - Spin-coated PMMA A3 950 (4000 rpm 40 s) - Baked at 180 °C 2 min - Spin-coated Espacer (4000 rpm 40s) - Patterned by e-beam lithography - Rinsed with DI water for 10 s + blow dry with N_2 gun - Developed for 30 s (MIBK:IPA=1:3) + IPA rinse + blow dry with N_2 gun - Ag 20 nm/Au 20 nm deposited by e-beam evaporation - Lift off in acetone (65 °C) + IPA rinse + blow dry with N_2 gun
6	Top gate dielectric

	- Deposited HfO_2 by ALD FIDJI (200 °C, 250 cycle)
7	Top gate - Spin-coated PMMA A4 950 (4000 rpm 40 s) - Baked at 180 °C 2 min - Spin-coated Espacer (4000 rpm 40 s) - Patterned by e-beam lithography - Rinsed with DI water for 10 s + blow dry with N_2 gun - Developed for 2 min (MIBK:IPA=1:3) + IPA rinse + blow dry with N_2 gun - Deposited Pd 40 nm by e-beam evaporation - Lift off in acetone (65 °C) + IPA rinse + blow dry with N_2 gun
8	Measurement

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